

# Q45T-AS

Rev: 1.0

\*

McCreary(Corporate) ,vPro
EagleLake Q: Corporate Integrated Graphics

Boulder Creek(consumer) ,VIIV
EagleLake G: Consumer Integrated Graphics
EagleLake P: Consumer Discrete Graphics

\*

PCB	Total Thickness	Core Prepreg
BearLake	62 mil	50 mil
EagleLake	59 mil	47 mil

www.aitech1.ru

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	E/F/G/H	PEQ1	GNT1
PCI2	18	F/G/H/E	PEQ0	GNT0

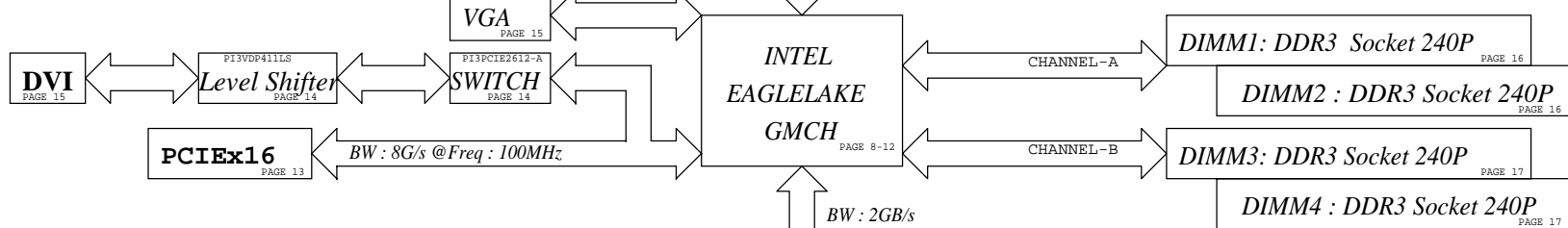
**INTEL  
LGA 775 pin**  
Intel P4 Processor Core 2 Duo  
& Core 2 Quad & Dual Core

PAGE 4-6

FSB : 800MHz & Freq : 200MHz  
FSB : 1066MHz & Freq : 266MHz  
FSB : 1333MHz & Freq : 333MHz

BW : 10GB/s

DDR3 : 800/1066/1333MHz  
BW:10.6G/s @DDR3 :1333MHz single-channel  
BW:21G/s @DDR3 :1333MHz dual-channel



BW : 480MB/s @ Freq : 48MHz

USBLAN  
2 ports  
USB X4  
4 ports  
USB3  
2 ports  
USB4  
2 ports

USB V2.0  
PAGE 25

**INTEL  
ICH9/10**

PAGE 19-22

BW : 500MB/s @ Freq : 100MHz

**PCIE X 1**

PAGE 26

**INTEL LAN  
82567LM  
(Giga PHY)**

PAGE 31

USBLAN  
RJ45

PAGE 31

**PCI Slot 120pin @ AD17**

PAGE 27

**PCI Slot 120pin @ AD18**

PAGE 27

BW : 133MB/s @ Freq : 33MHz

PS. USBLAN is RJ45+2 port USB conn

Mic In  
Line Out  
Line In

**HD Audio  
Codec  
ALC662**

PAGE 32

SATA1 7Pin

SATA2 7pin

SATA3 7Pin

E-SATA6 7pin

SATA-II  
BW : 3G/s

PAGE 26

**SPI ROM**

PAGE 23

**ITE 8720  
Super I/O**

PAGE 28

**FLOPPY**

PAGE 28

**LPT**

PAGE 28

**COM X 2**

PAGE 28

**TPM**

PAGE 24

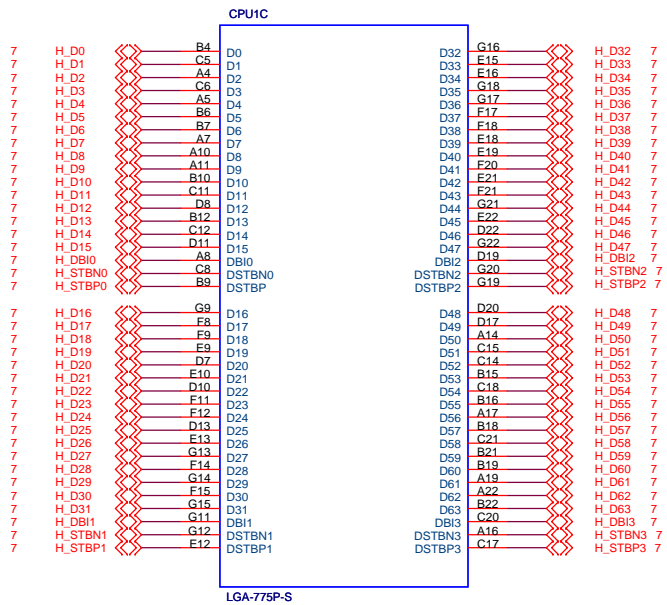
#### Design\_Guide\_Rev1\_1\_1

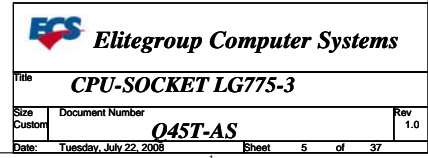
ICH10	Consumer	Corporate
GP8	DDR3_PWR-OK	Unmuxed.
GP58	Not available.	SEI CS1
GP10	CPU_MISSING	Not available.
GP15	CK_PCISTOP	May be left unconnected.
GP25	CK_CPUSTOP	May be left unconnected.

PCB : 244 x 244 x 1.6 mm ; 4 layers

<b>System Block Diagram</b>			
Size	Document Number	Rev	
Custom	<b>Q45T-AS</b>	1.0	
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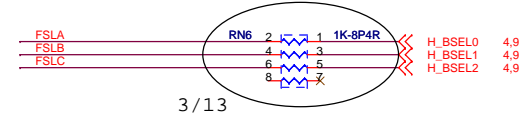
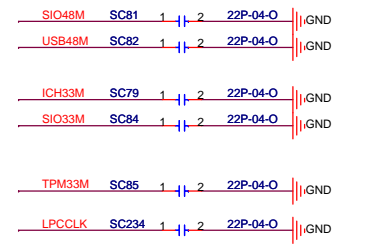
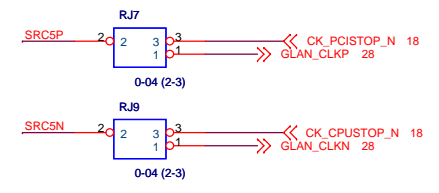
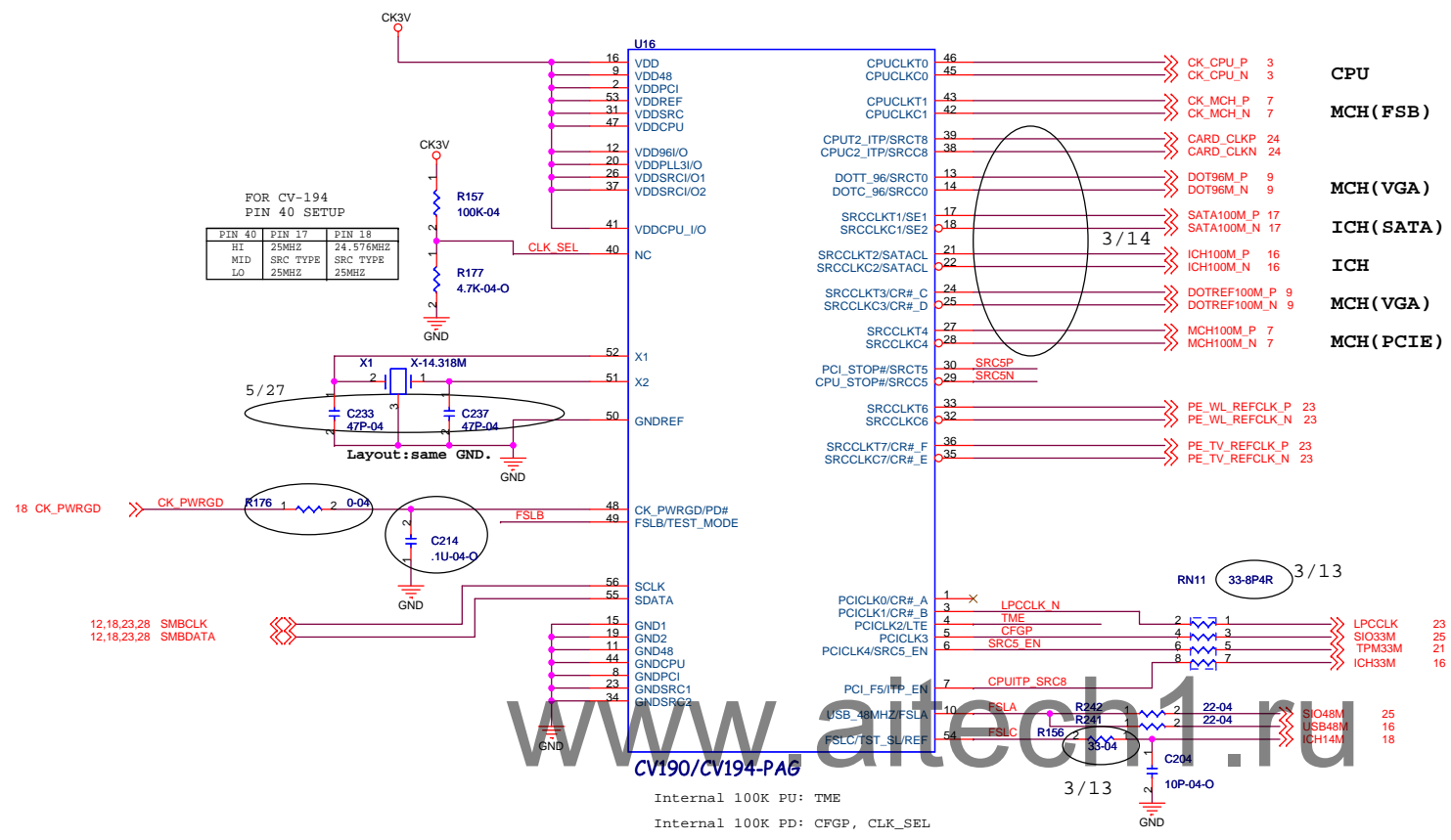




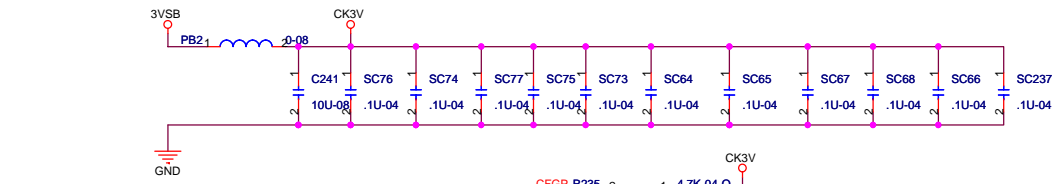


FOR CV-194  
PIN 40 SETUP

PIN 40	PIN 17	PIN 18
HI	25MHZ	24.576MHZ
MID	SRC TYPE	SRC TYPE
LO	25MHZ	25MHZ



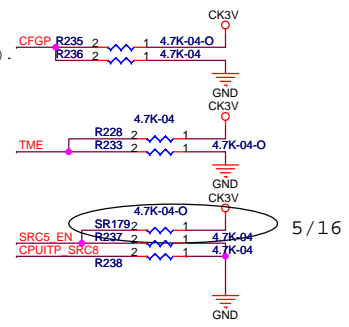
Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU CLOCK (MHZ)
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00



High, SATA from PLL2. Low, SATA from PLL4 (as SRC clock).

High, internal 33 ohm resistor enabled. Low, disabled.

High = SRC5, Low = CPU and PCI Stop#.  
High = CPU\_ITP, Low = SRC8.

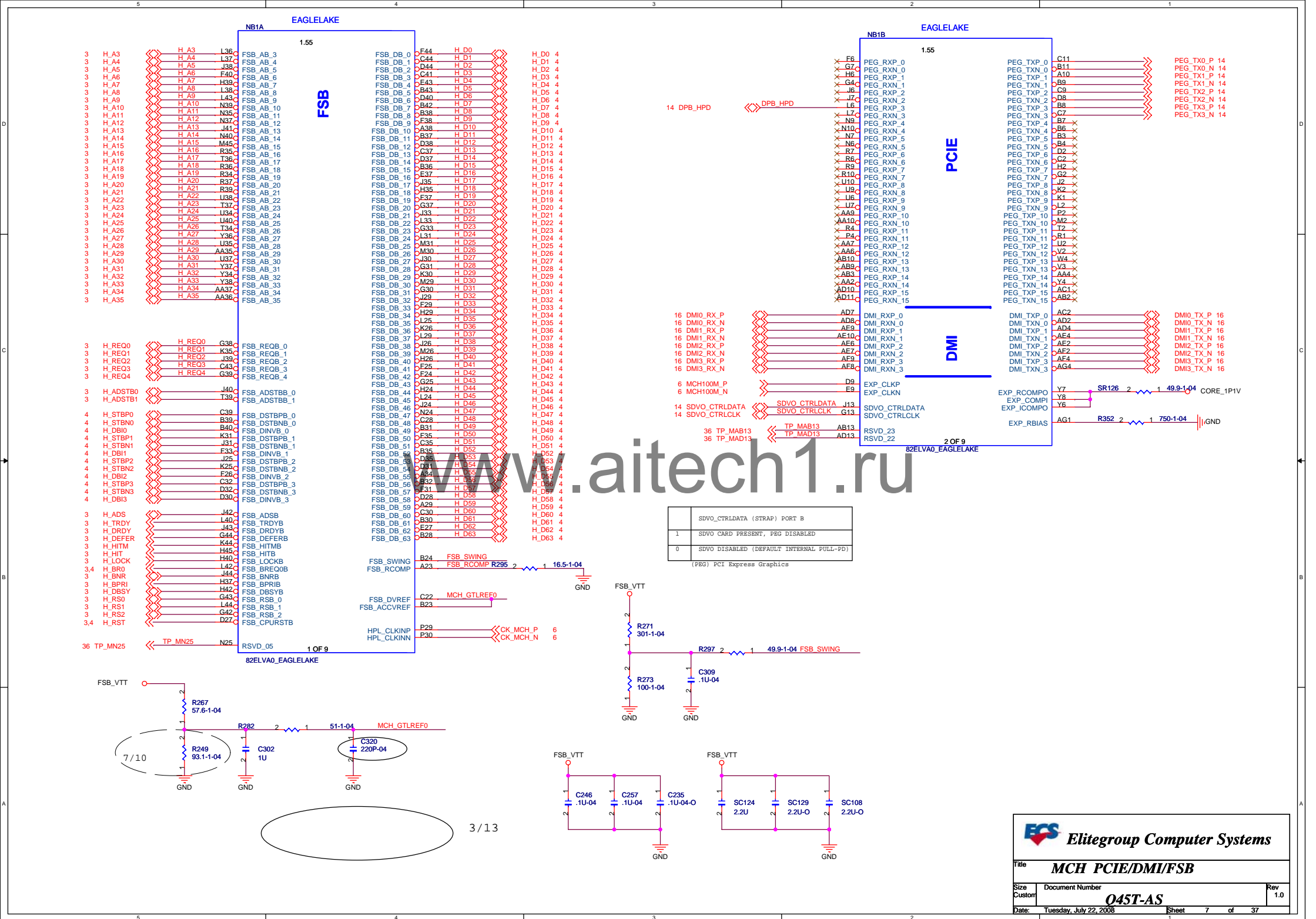


**Elitegroup Computer Systems**

Title: **CV190/CV194**

Size Custom: Document Number: **Q45T-AS** Rev: 1.0

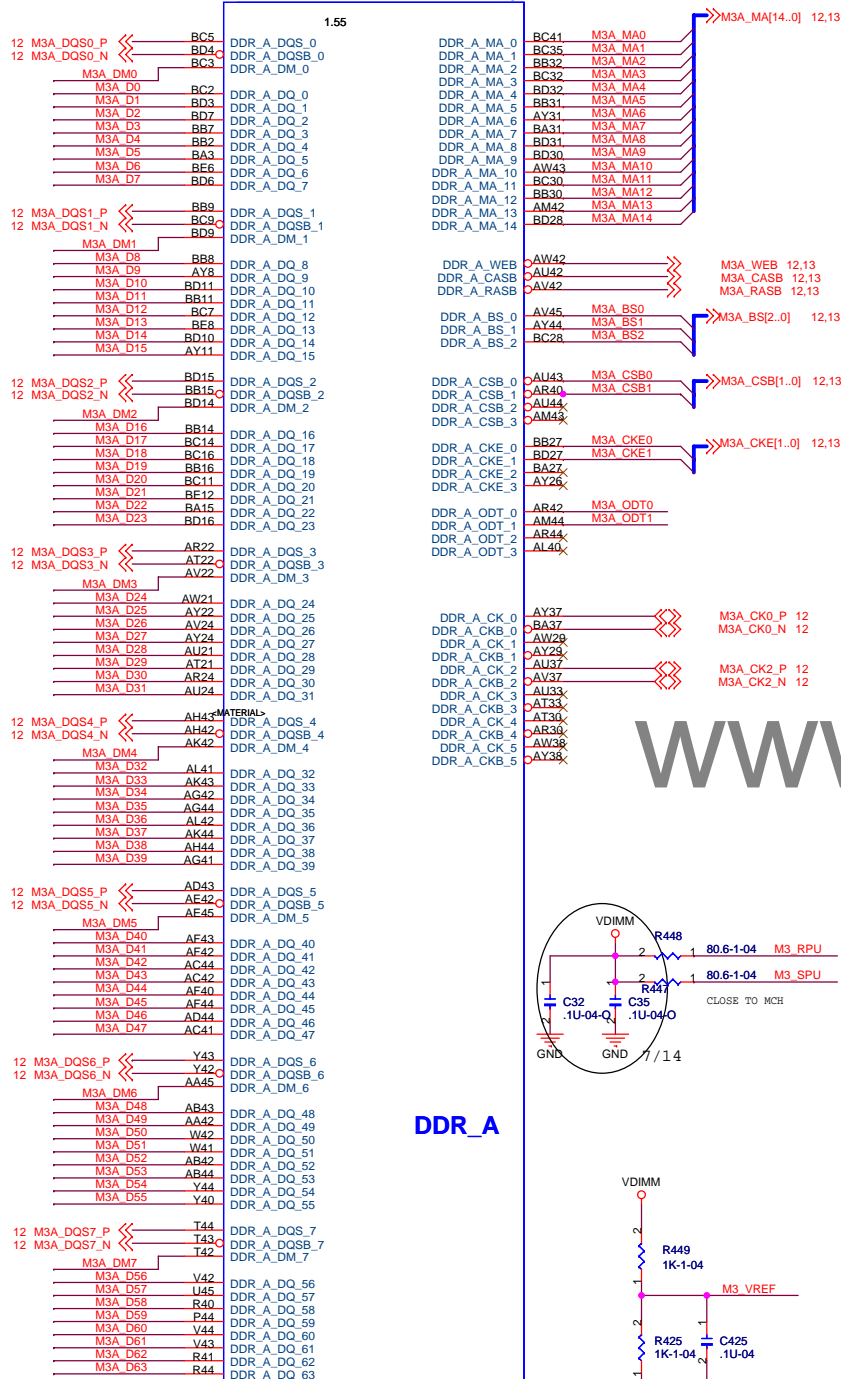
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## EAGLELAKE

NB1C

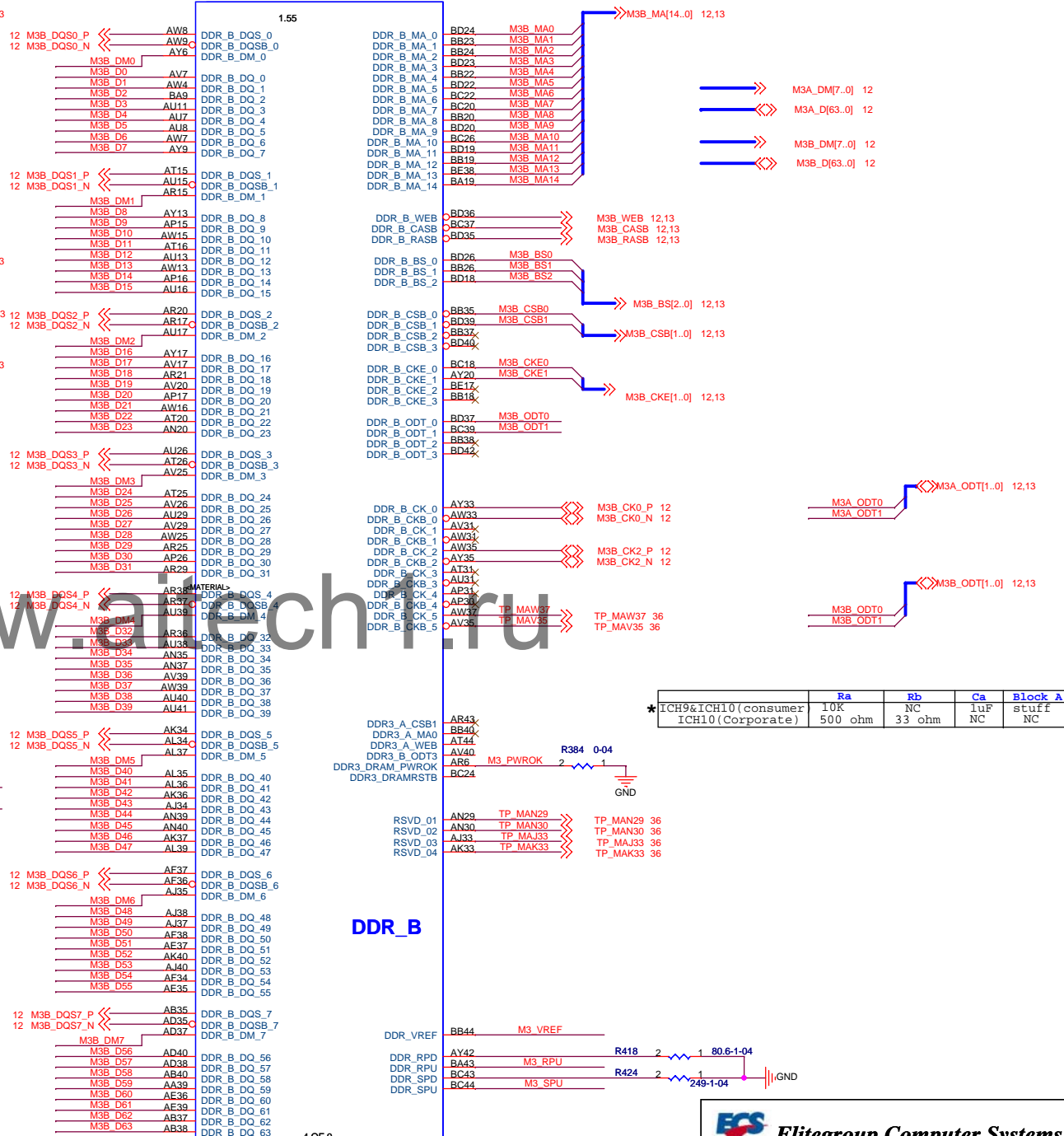


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82ELVA0\_EAGLELAKE

## EAGLELAKE

NB1D



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82ELVA0\_EAGLELAKE

	Ra	Rb	Ca	Block A
* ICH9&ICH10 (consumer)	10K	NC	1uF	stuff
ICH10 (Corporate)	500 ohm	33 ohm	NC	NC



Elitegroup Computer Systems

Title MCH /DDRIII/DDRII2

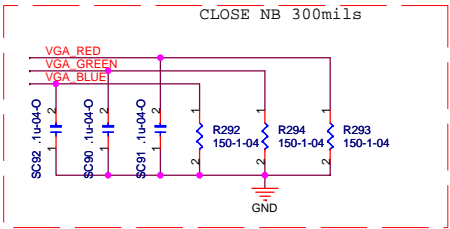
Size Custom Document Number Q45T-AS


Rev 1.0

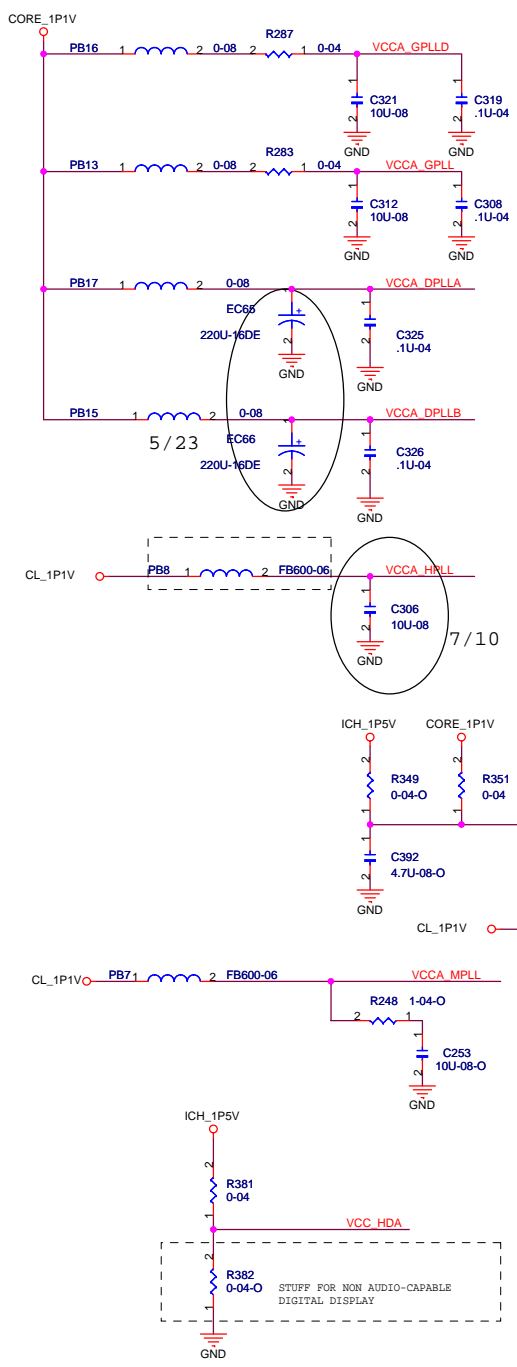
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 <b>Elitegroup Computer Systems</b>				
Title <b>MCH /VGA/MISC</b>				
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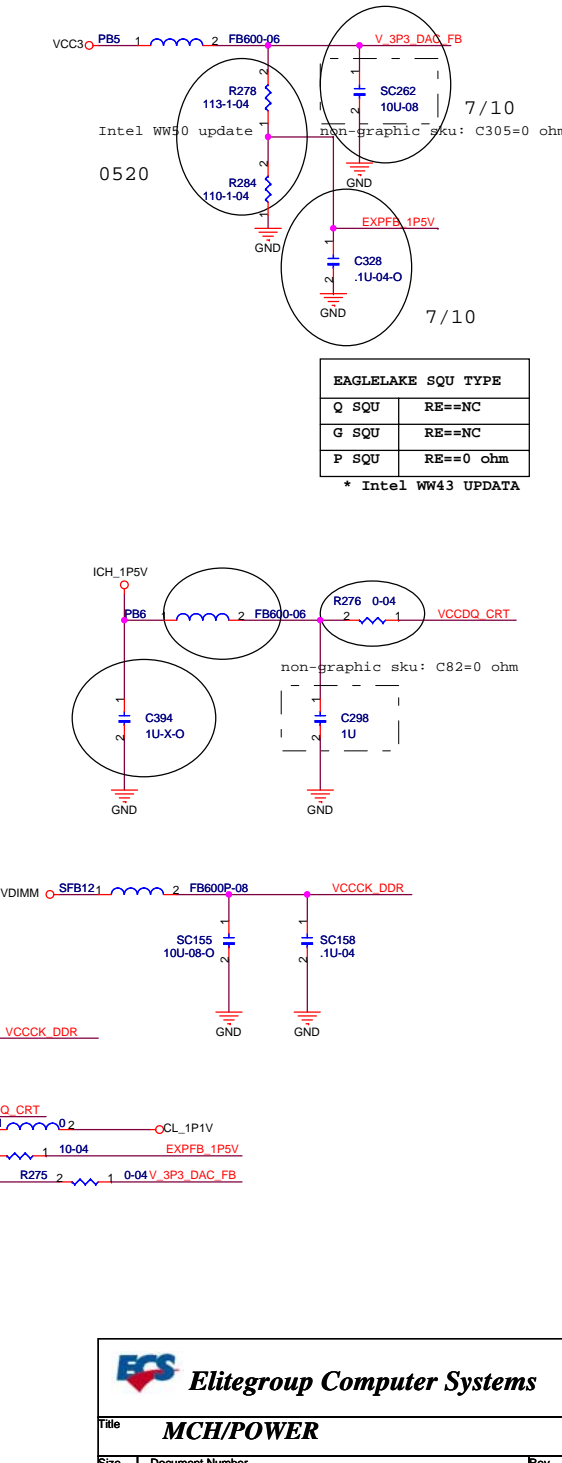
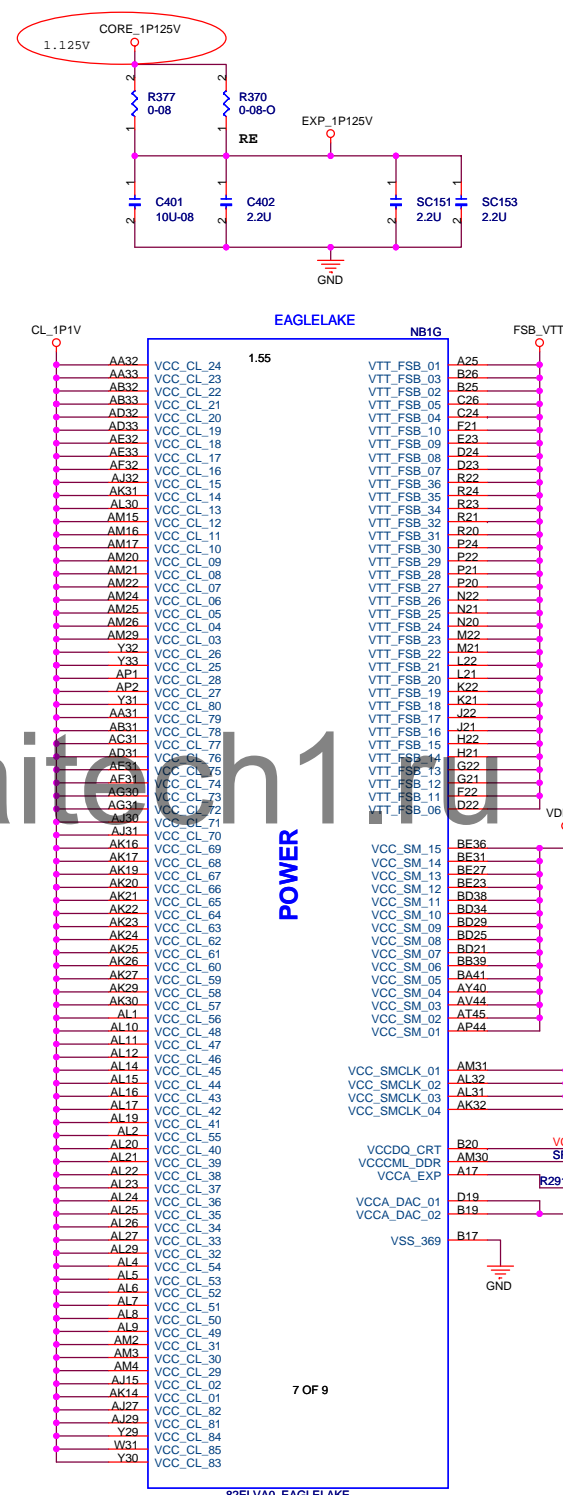


**EAGLELAKE**

EXP_1P125V	1.55	VCC_EXP_2	VCC_01	AA19	CORE_1P1V
AJ2	VCC_EXP_1	VCC_02	AA21		
AJ1	VCC_EXP_34	VCC_03	AA23		
Y14	VCC_EXP_35	VCC_04	AA25		
W15	VCC_EXP_36	VCC_05	AA27		
U15	VCC_EXP_37	VCC_06	AA29		
U14	VCC_EXP_06	VCC_07	AA30		
AK9	VCC_EXP_10	VCC_08	AB20		
AK8	VCC_EXP_11	VCC_09	AB22		
AK7	VCC_EXP_12	VCC_10	AB24		
AK6	VCC_EXP_13	VCC_11	AB26		
AK13	VCC_EXP_06	VCC_12	AB29		
AK12	VCC_EXP_07	VCC_13	AB30		
AK11	VCC_EXP_08	VCC_14	AC16		
AK10	VCC_EXP_09	VCC_15	AC17		
AJ9	VCC_EXP_19	VCC_16	AD33		
AJ8	VCC_EXP_20	VCC_17	AD32		
AJ7	VCC_EXP_21	VCC_18	AE32		
AJ6	VCC_EXP_22	VCC_19	AE33		
AJ14	VCC_EXP_14	VCC_20	AE32		
AJ13	VCC_EXP_15	VCC_21	AE32		
AJ12	VCC_EXP_16	VCC_22	AD16		
AJ11	VCC_EXP_17	VCC_23	AD17		
AJ10	VCC_EXP_18	VCC_24	AD20		
AG15	VCC_EXP_23	VCC_25	AD22		
AF15	VCC_EXP_24	VCC_26	AD24		
AF14	VCC_EXP_25	VCC_27	AM20		
AF13	VCC_EXP_26	VCC_28	AM21		
AD15	VCC_EXP_27	VCC_29	AE16		
AD14	VCC_EXP_28	VCC_30	AE17		
AD13	VCC_EXP_29	VCC_31	AE19		
AD12	VCC_EXP_30	VCC_32	AE21		
AD11	VCC_EXP_31	VCC_33	T23		
AD10	VCC_EXP_32	VCC_34	T22		
AA15	VCC_EXP_33	VCC_35	AE23		
AK3	VCC_EXP_4	VCC_36	AE25		
AK4	VCC_EXP_5	VCC_37	AP2		
AK2	VCC_EXP_3	VCC_38	Y32		
		VCC_39	Y33		
		VCC_40	Y32		
		VCC_41	Y33		
		VCC_42	Y32		
		VCC_43	Y33		
		VCC_44	Y32		
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		VCC_90	Y32		
		VCC_91	Y33		

**POWER**

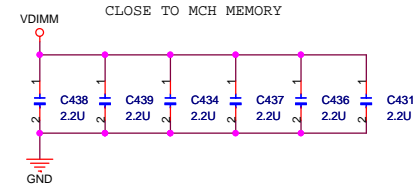
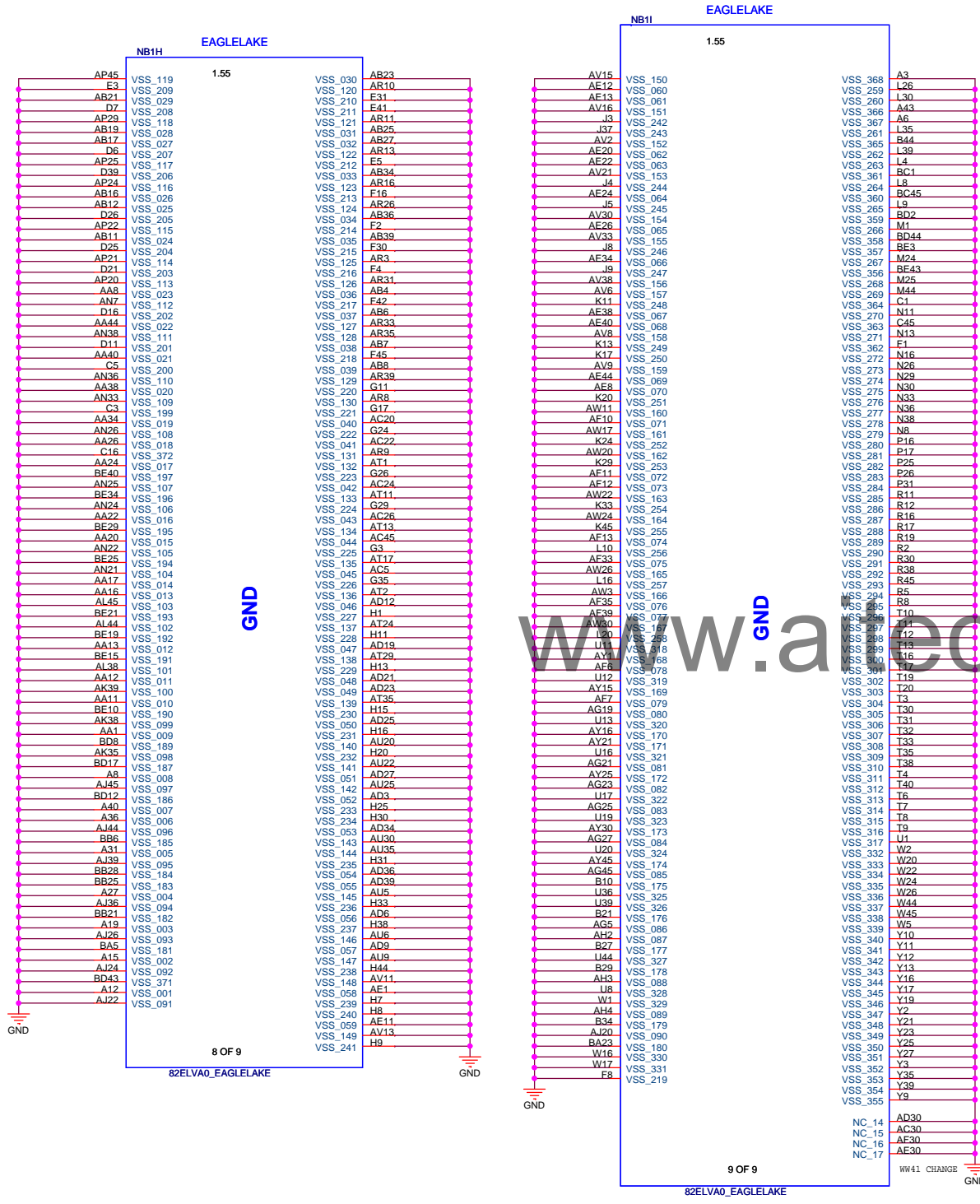
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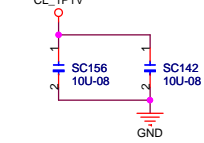
**EAGLELAKE SQU TYPE**

Q SQU	RE==NC
G SQU	RE==NC
P SQU	RE==0 ohm

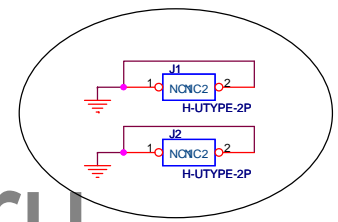
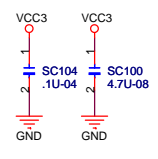
\* Intel WW43 UPDATA



ME DECOUPLING

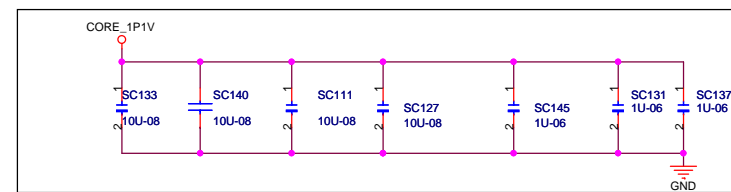


VCC\_HVGIO DECOUPLING

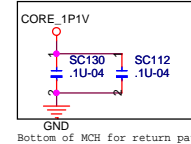
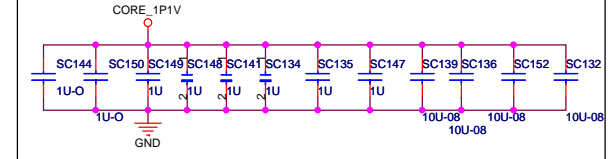


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Edge of MCH



Bottom of MCH



**Elitegroup Computer Systems**

Title: **MCH /GND**

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8,13 M3A\_MA[14..0] << M3A\_MA[14..0]  
8,13 M3A\_BS[2..0] << M3A\_BS[2..0]  
8 M3A\_DM[7..0] << M3A\_DM[7..0]

VDIMM

M3A\_D[63..0] << M3A\_D[63..0] 8

8 M3B\_DM[7..0] << M3B\_DM[7..0]  
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VDIMM

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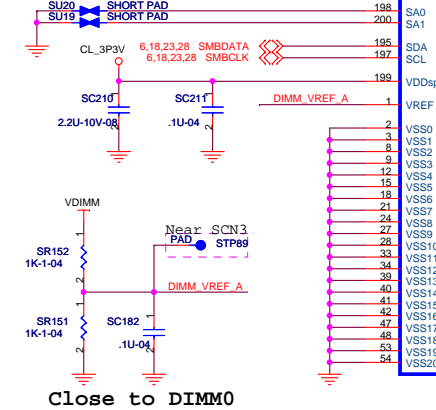
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M3A MA7 95 A7  
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M3A MA9 93 A9  
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M3A MA11 91 A11  
M3A MA12 90 A12  
M3A MA13 89 A13  
M3A MA14 88 A14  
M3A BS0 107 BA0  
M3A BS1 106 BA1  
M3A BS2 105 BA2  
M3A DM0 10 DM0  
M3A DM1 26 DM1  
M3A DM2 52 DM2  
M3A DM3 67 DM3  
M3A DM4 130 DM4  
M3A DM5 147 DM5  
M3A DM6 170 DM6  
M3A DM7 185 DM7

5 M3A D0 D00  
7 M3A D1 D01  
17 M3A D2 D02  
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194 M3A D63 D063

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8 M3A DQ0\_S N 31 DQS1  
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8 M3A DQ0\_S6 P 169 DQS6  
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8 M3A DQ0\_S7\_N 186 DQS7  
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8,13 M3A\_CKE0 79 CKE0  
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SO-DIMM

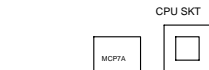
9.2H



Close to DIMM0

SMBus Addressing

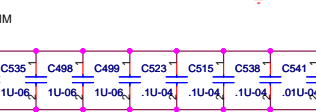
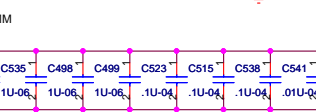
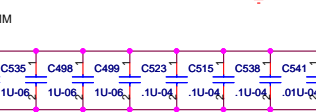
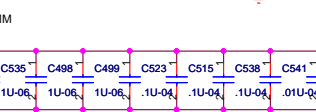
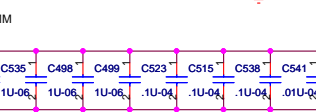
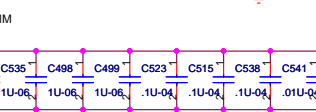
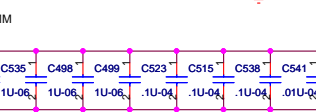
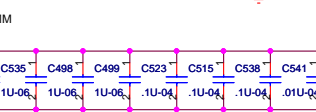
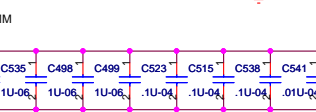
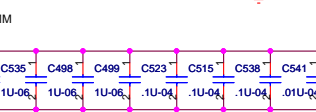
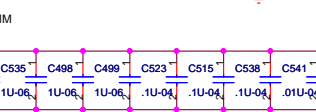
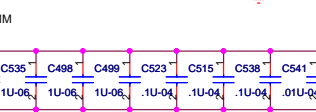
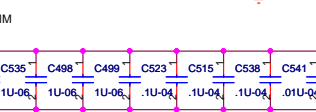
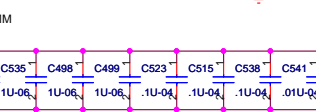
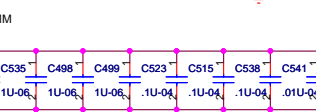
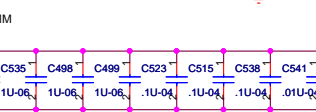
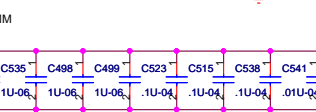
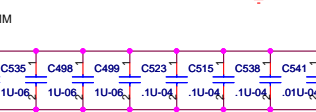
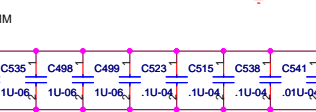
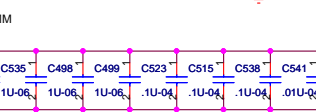
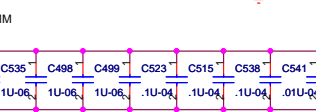
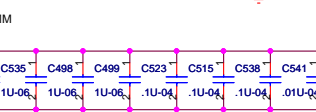
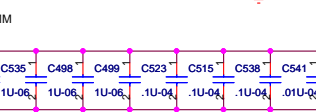
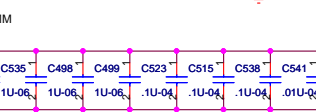
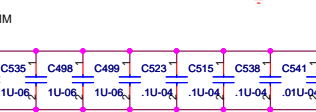
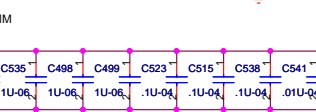
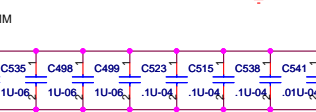
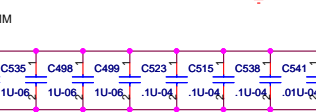
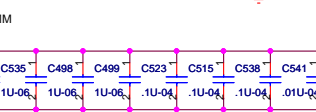
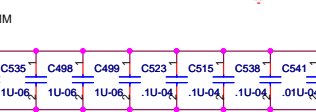
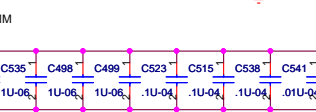
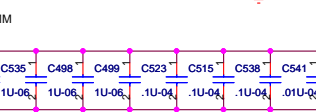
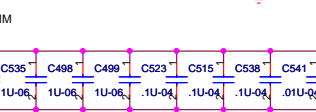
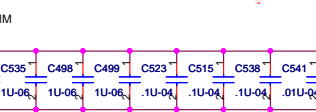
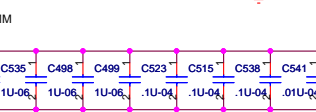
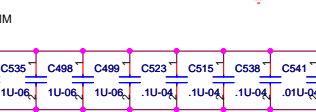
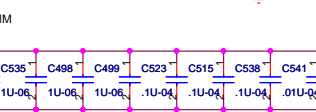
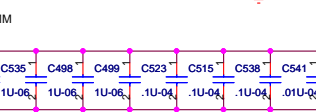
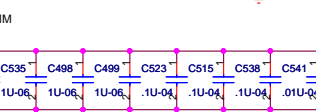
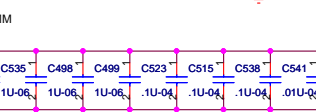
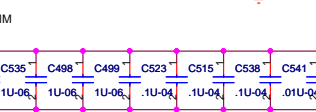
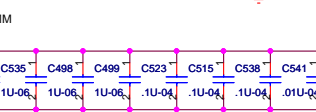
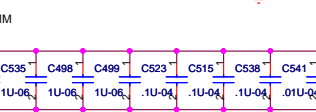
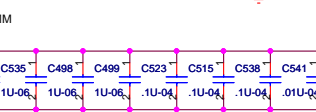
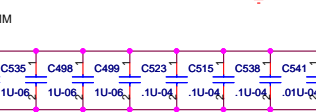
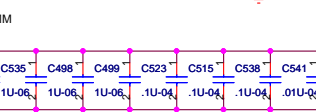
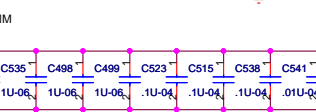
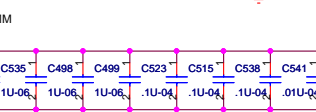
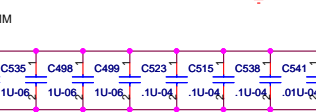
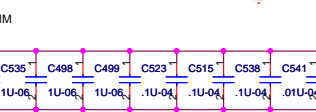
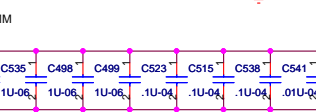
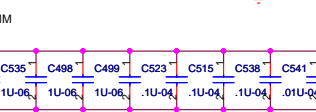
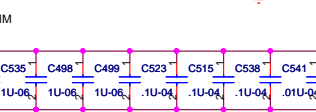
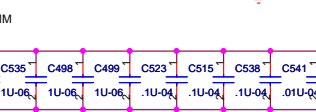
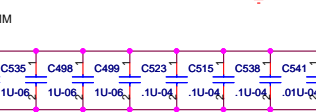
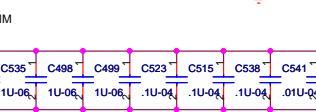
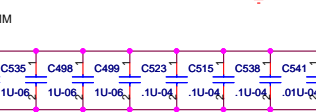
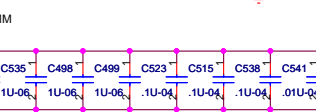
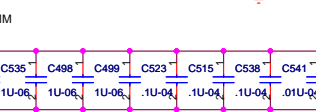
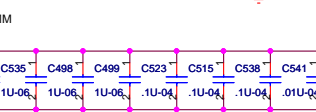
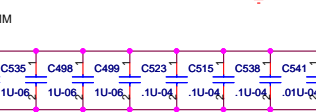
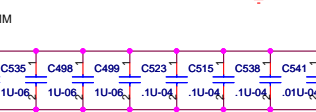
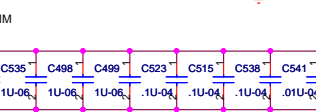
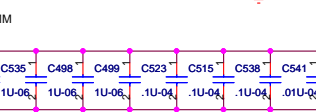
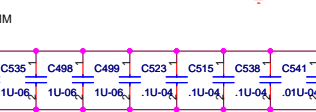
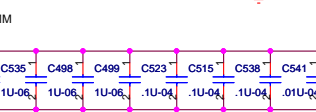
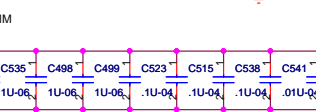
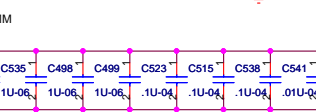
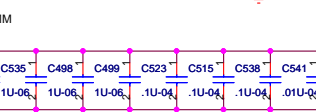
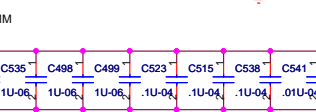
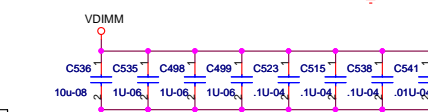
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2

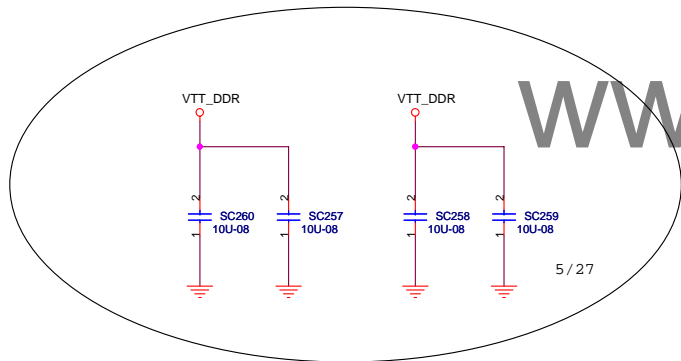


DATA 1 DIMM 1 ADDR 1/CNTL 1A  
DATA 0 DIMM 0 ADDR 0/CNTL 0A

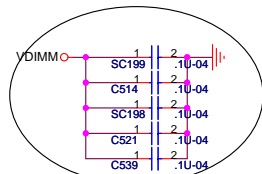
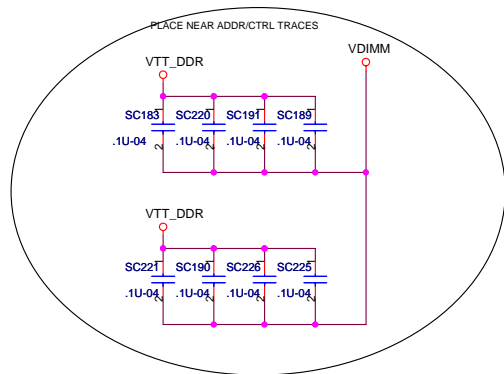
SM MEM BUS ADDRESS	
DIMM 0	1010 000
DIMM 1	1010 001

Close to DIMM1

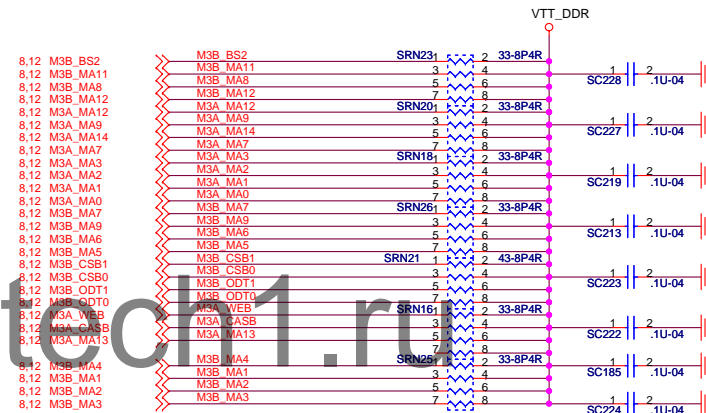
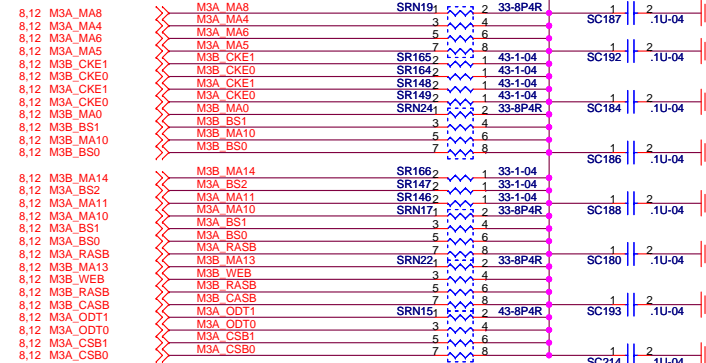
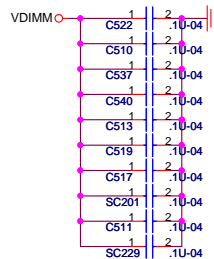
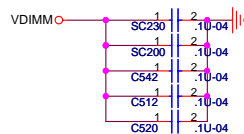




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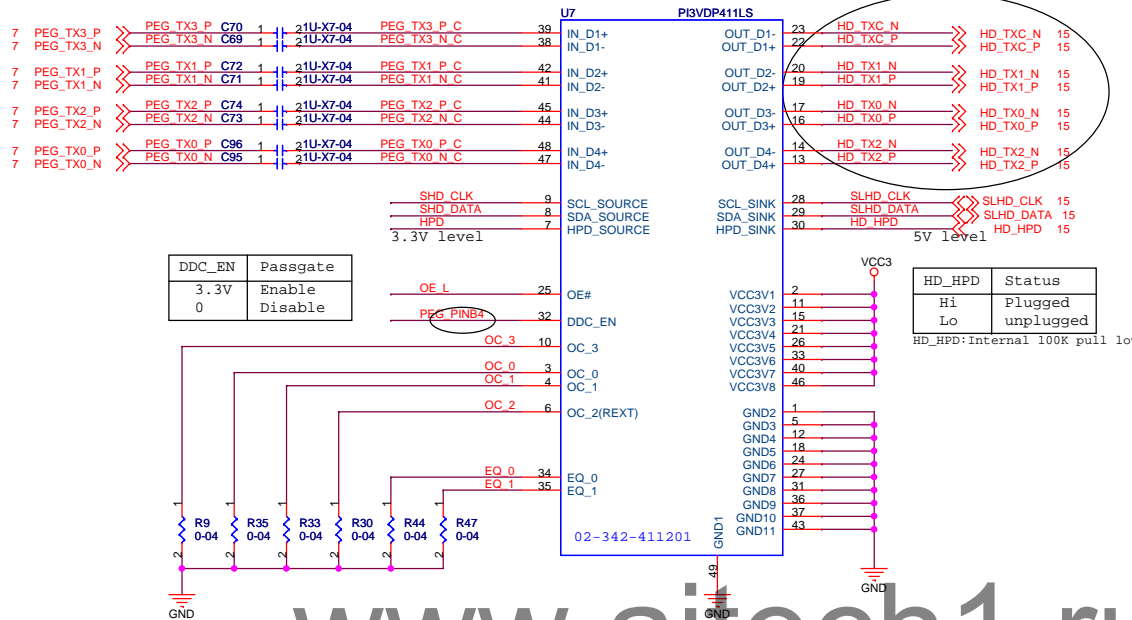


EMI decoupling cap. place evenly around CPU\_VDDIO\_SUS

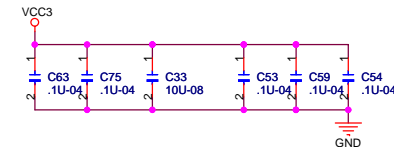
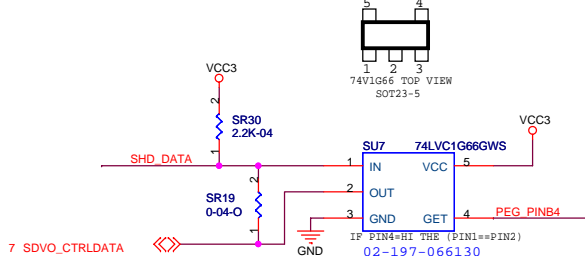
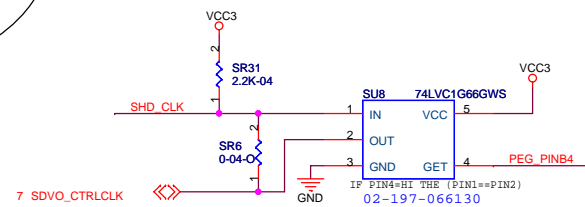
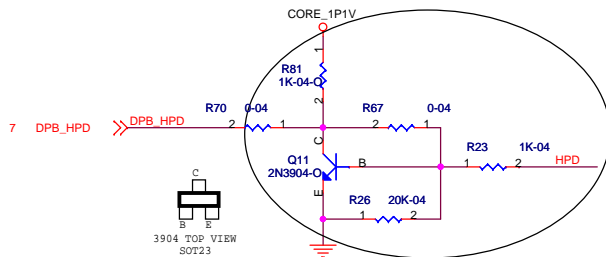


# Level Shifter

0520

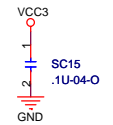


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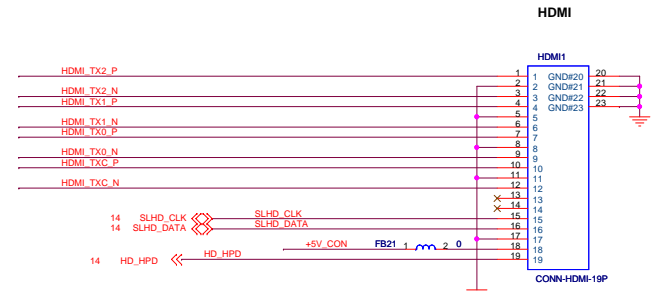
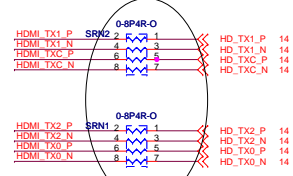
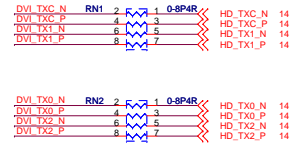
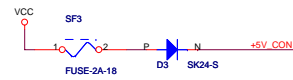
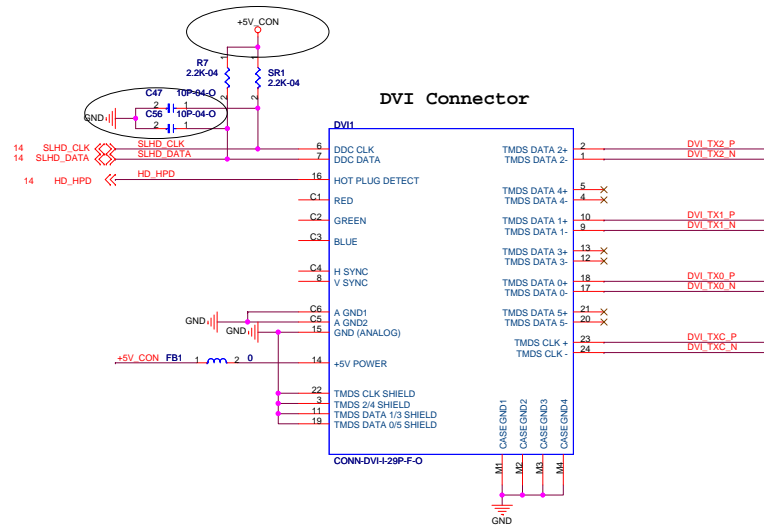


OC_3	OC_2	OC_1	OC_0	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
.	.	.	.	.	.

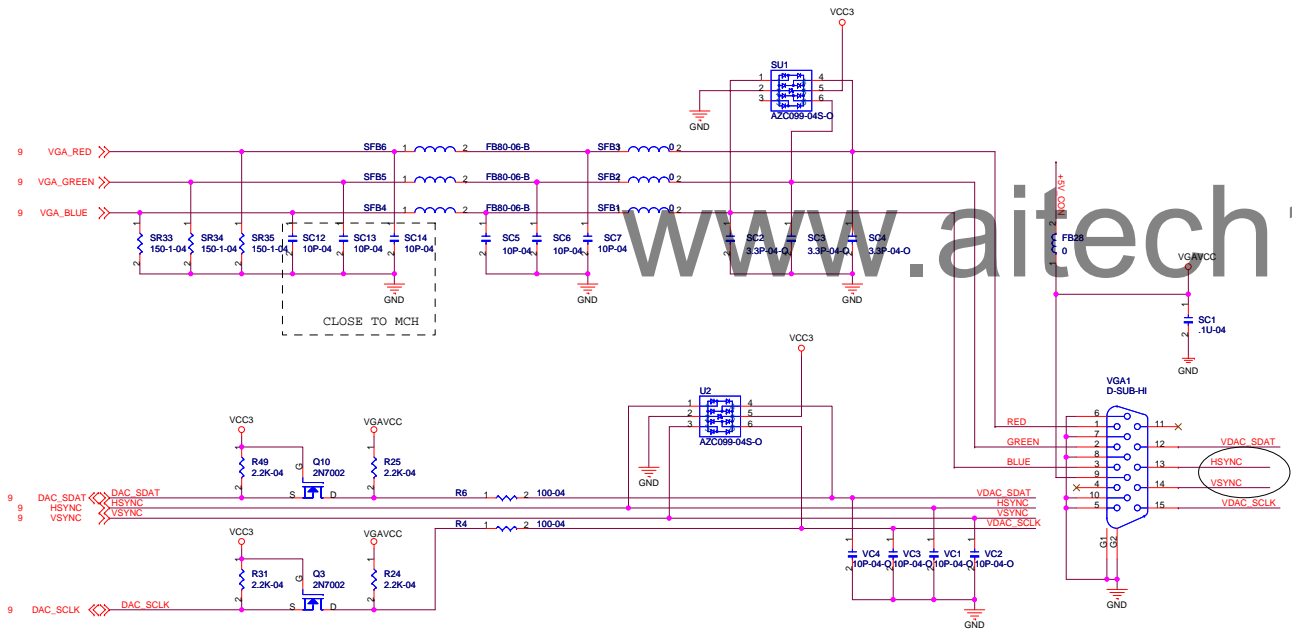
EQ_0	EQ_1	Equalization (dB)
0	0	3
0	1	7
1	0	10
1	1	20



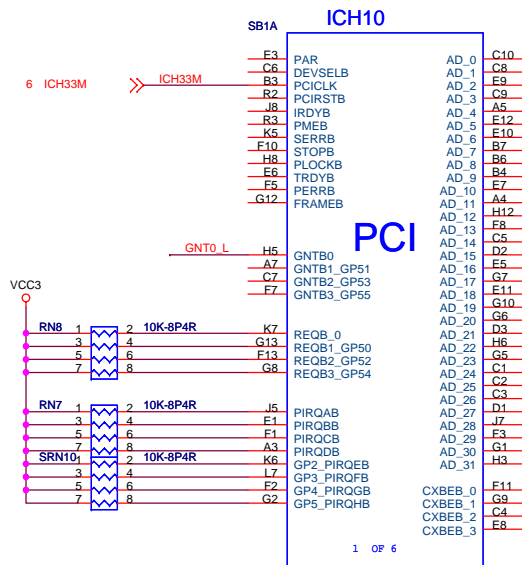




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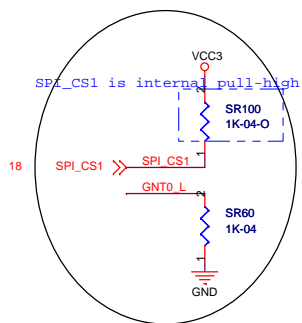
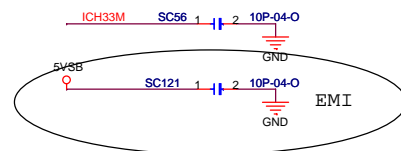
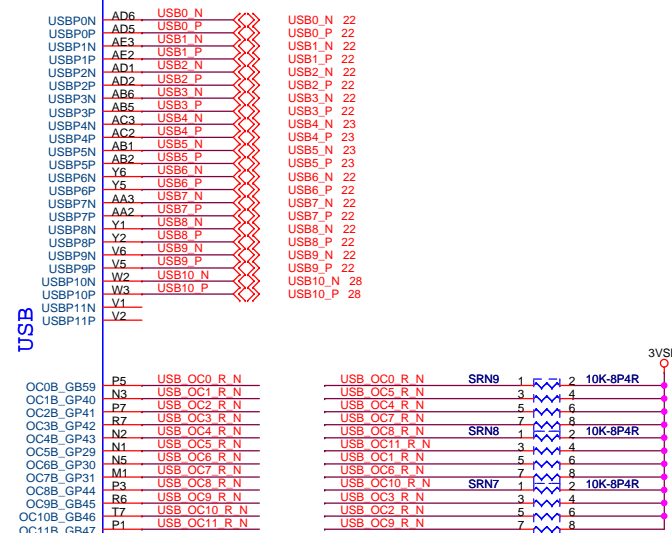
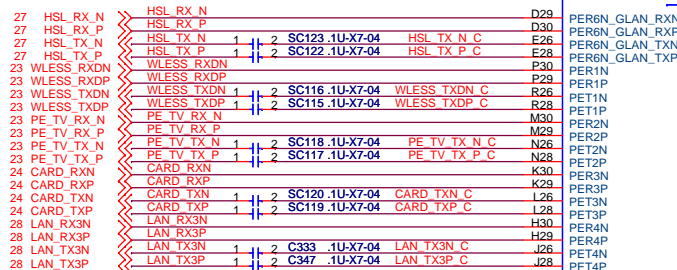






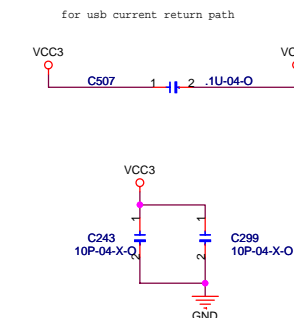
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BOOT BIOS DESTINATION SELECTION		
GNT0_L	SPI_CS1	BOOT BIOS DESTINATION
0	1	SPI
1	0	PCI
1	1	LPC
0	0	Reserved

\*Default

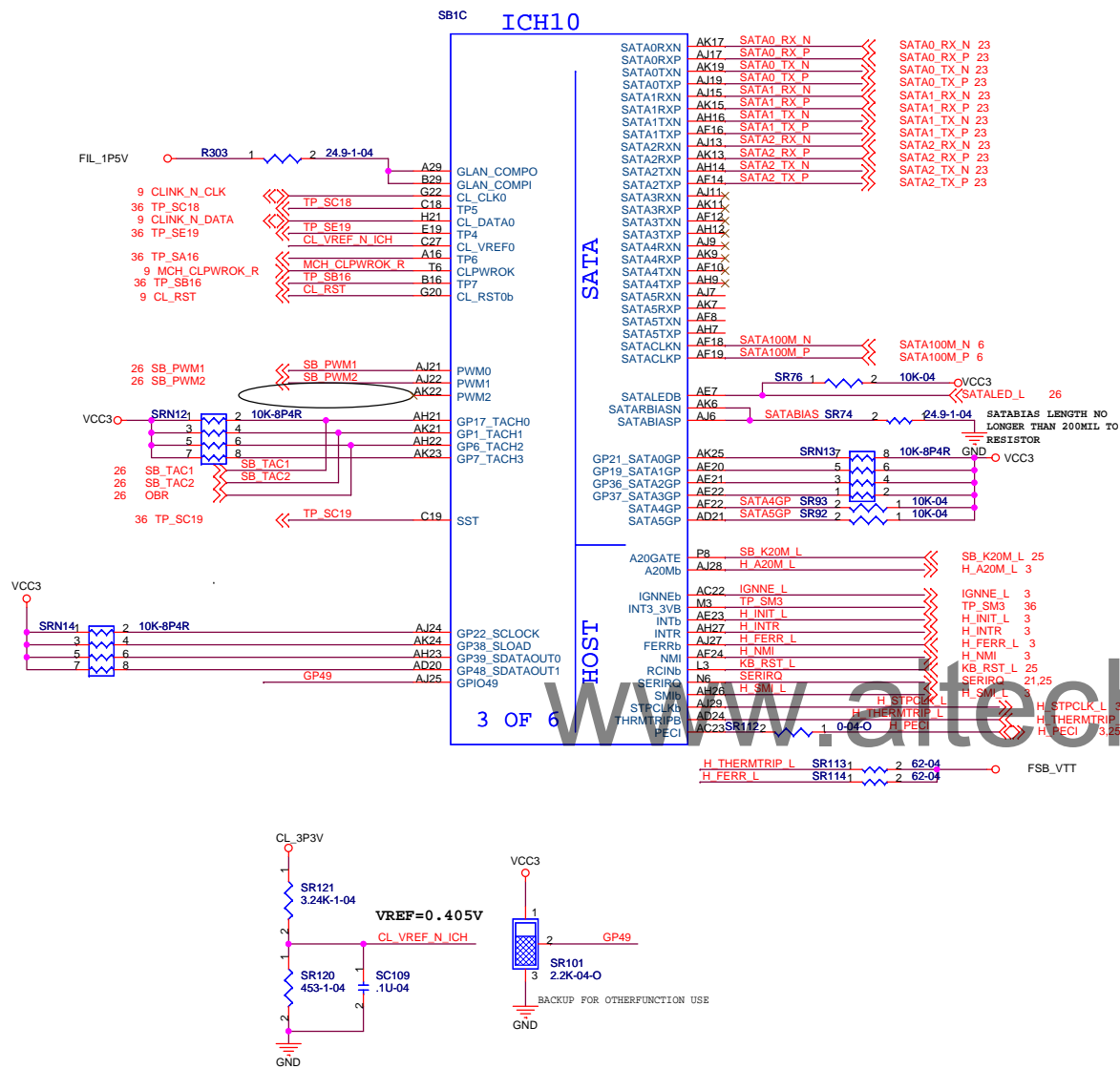


Elitegroup Computer Systems

Title ICH9/10 PCI/PCI-E

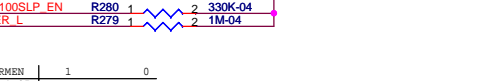
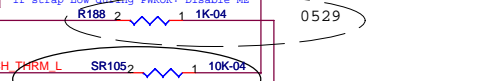
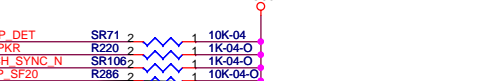
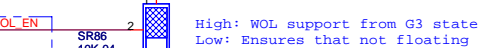
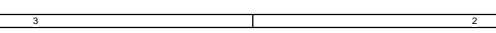
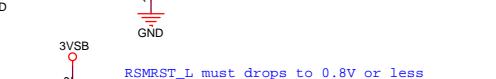
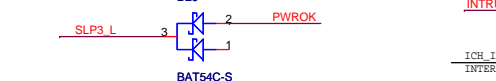
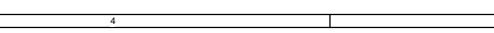
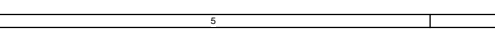
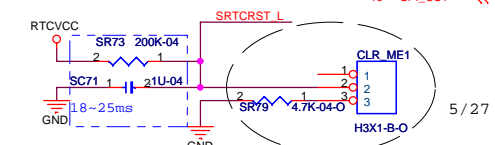
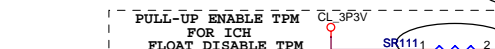
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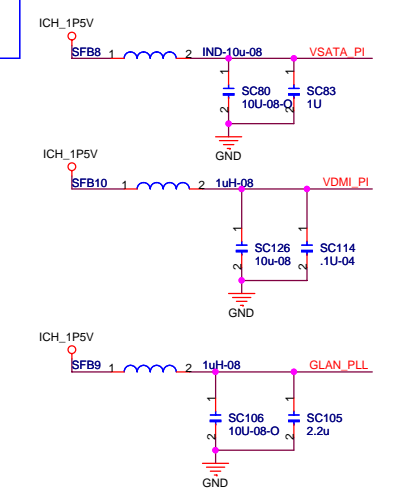
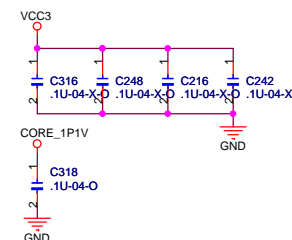
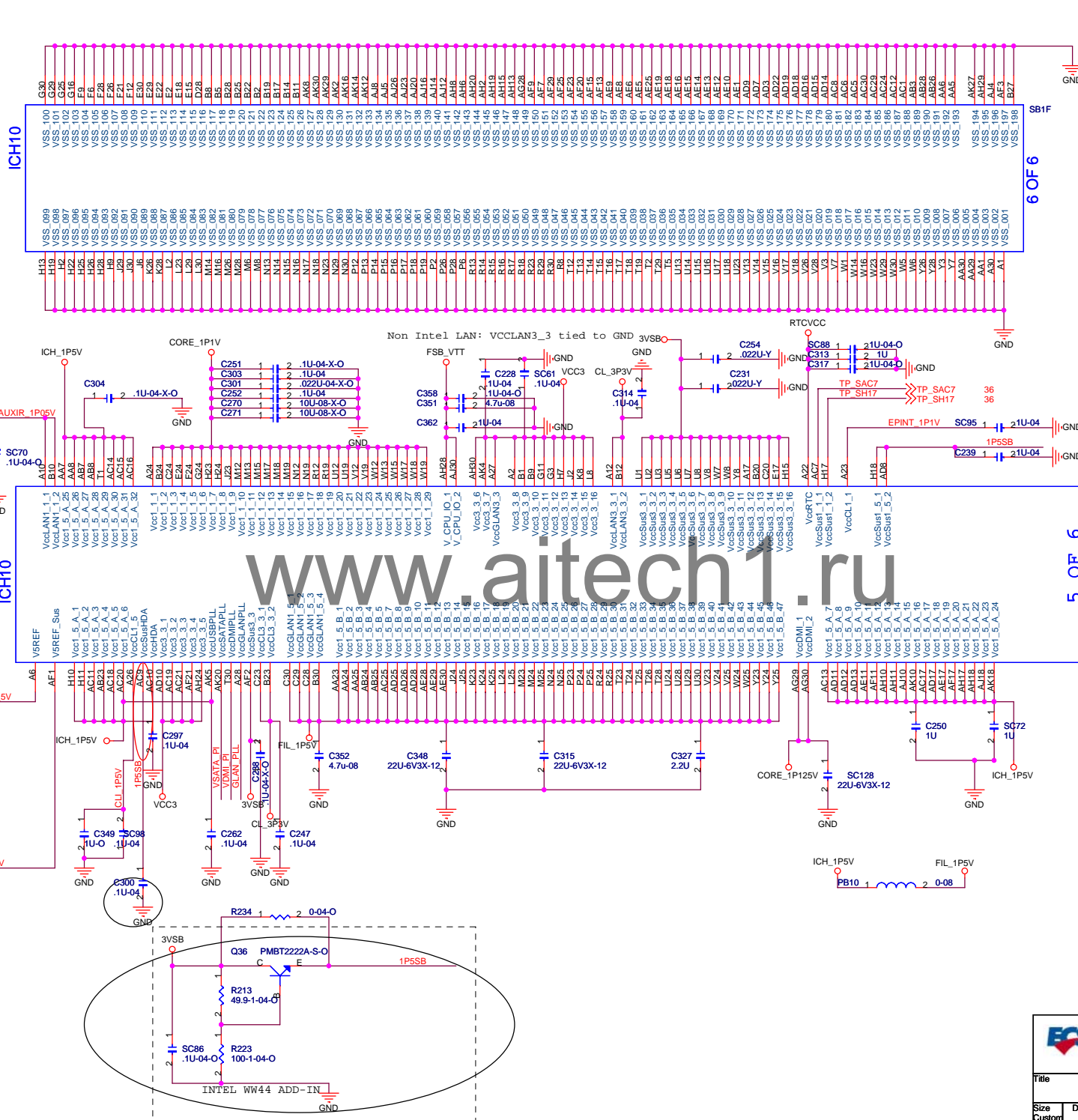
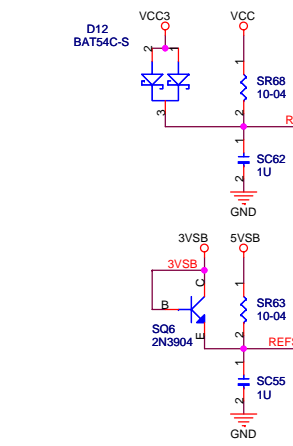
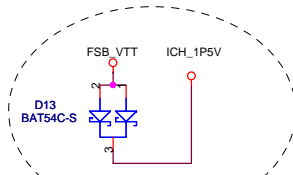
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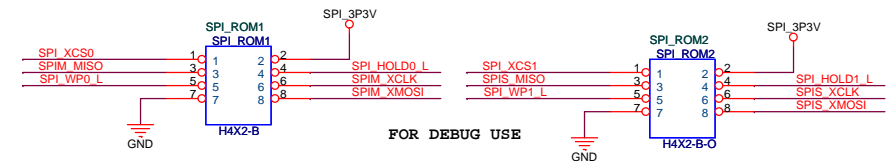
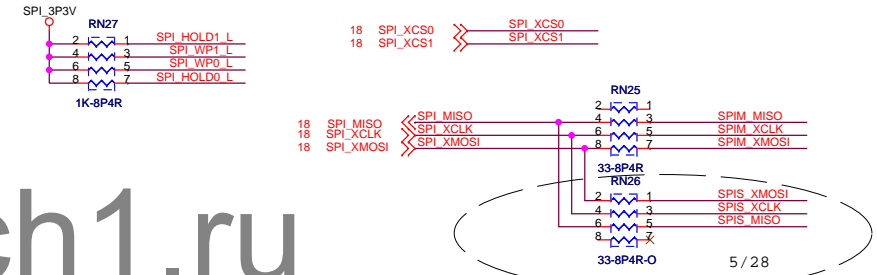
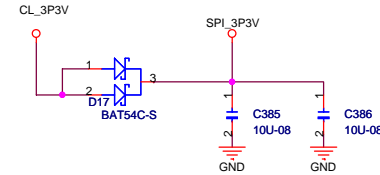
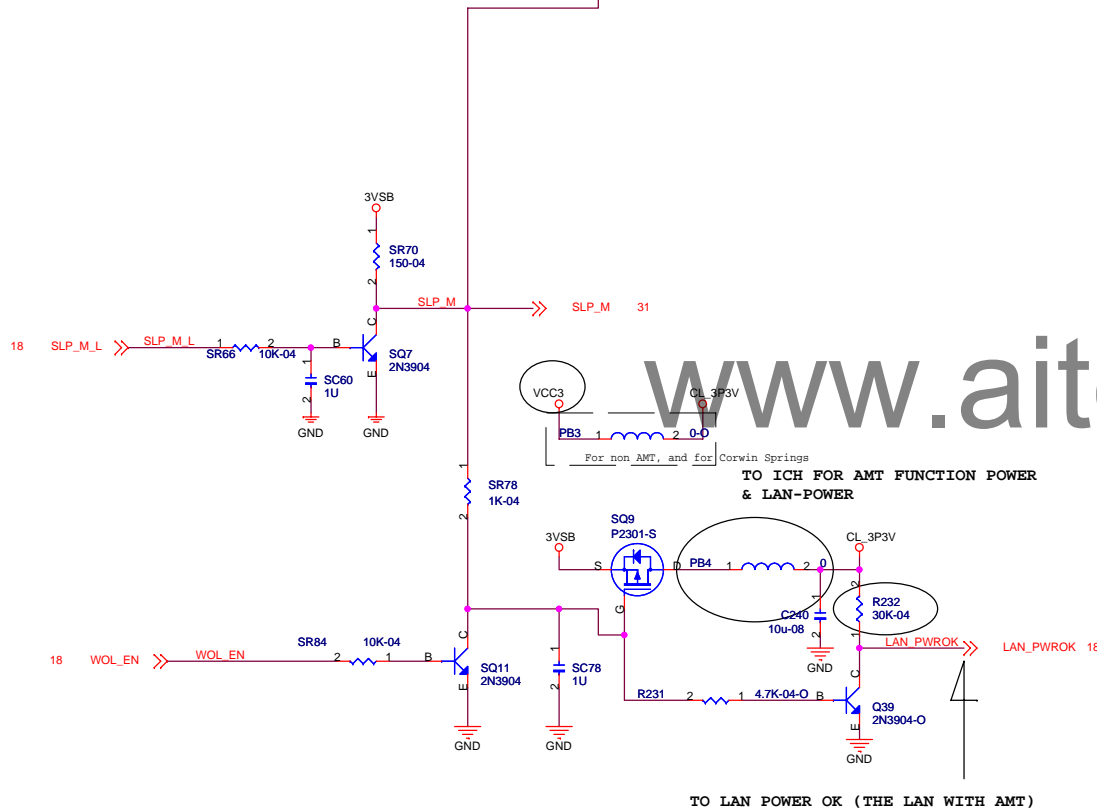
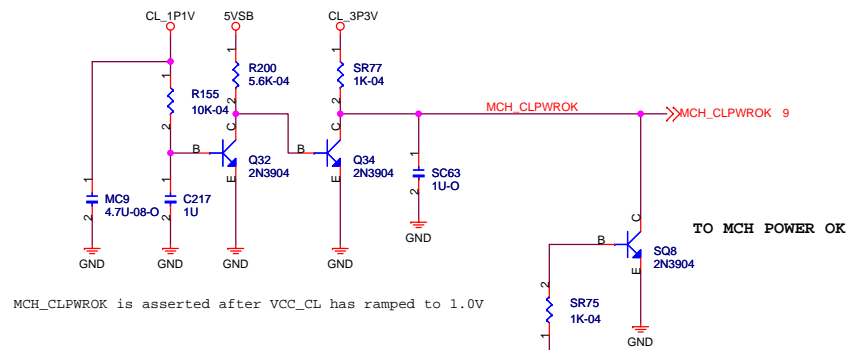


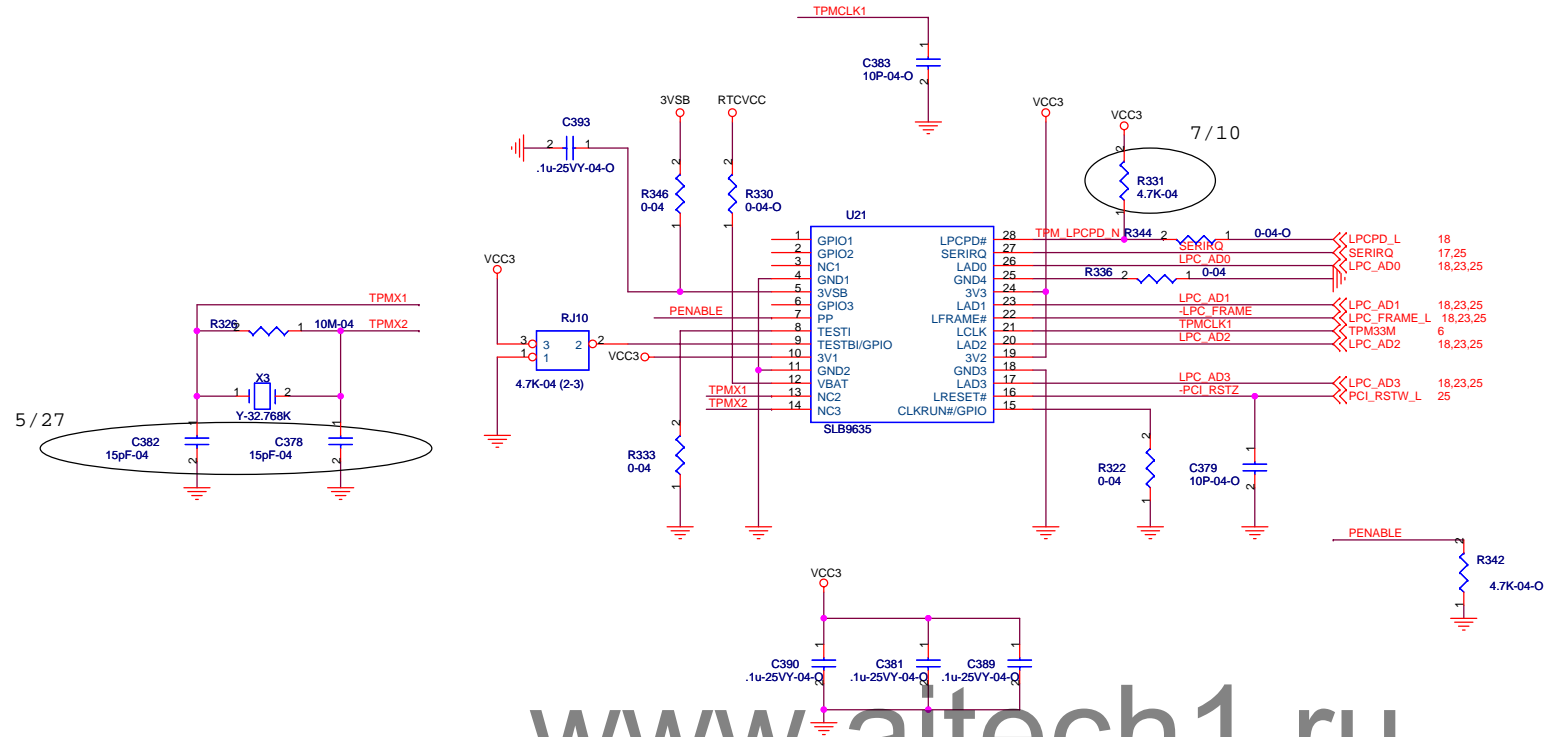
If without use pins L3,P8,N6  
Please (4.7K-10K) pull-up to VCC.  
Don't let it floating

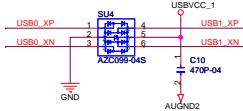
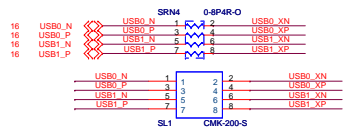
	ICH 10,C12 pin	ICH 10,C26 pin	MCH,L17 pin
Disable	Pulldown	Float	Float
Enable	Pullhi	Pullhi	Pulldown



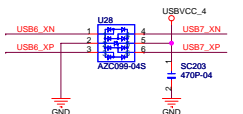
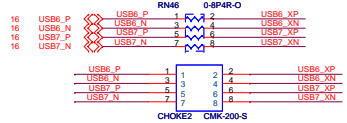
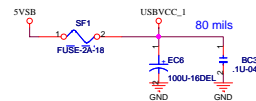
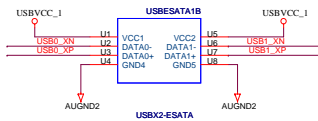




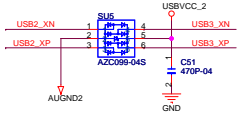
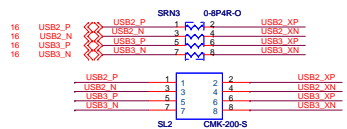
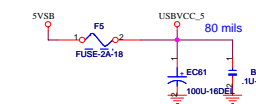
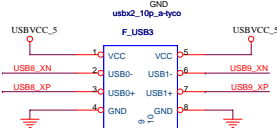
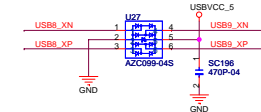
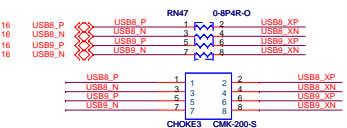
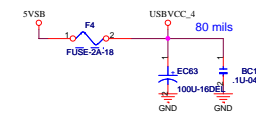
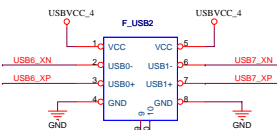




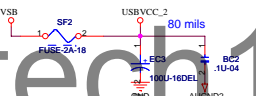
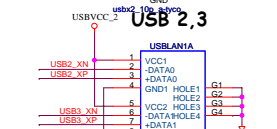
## USB 0,1



## USB 6,7

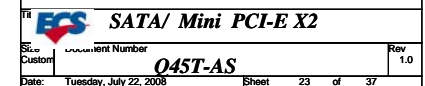


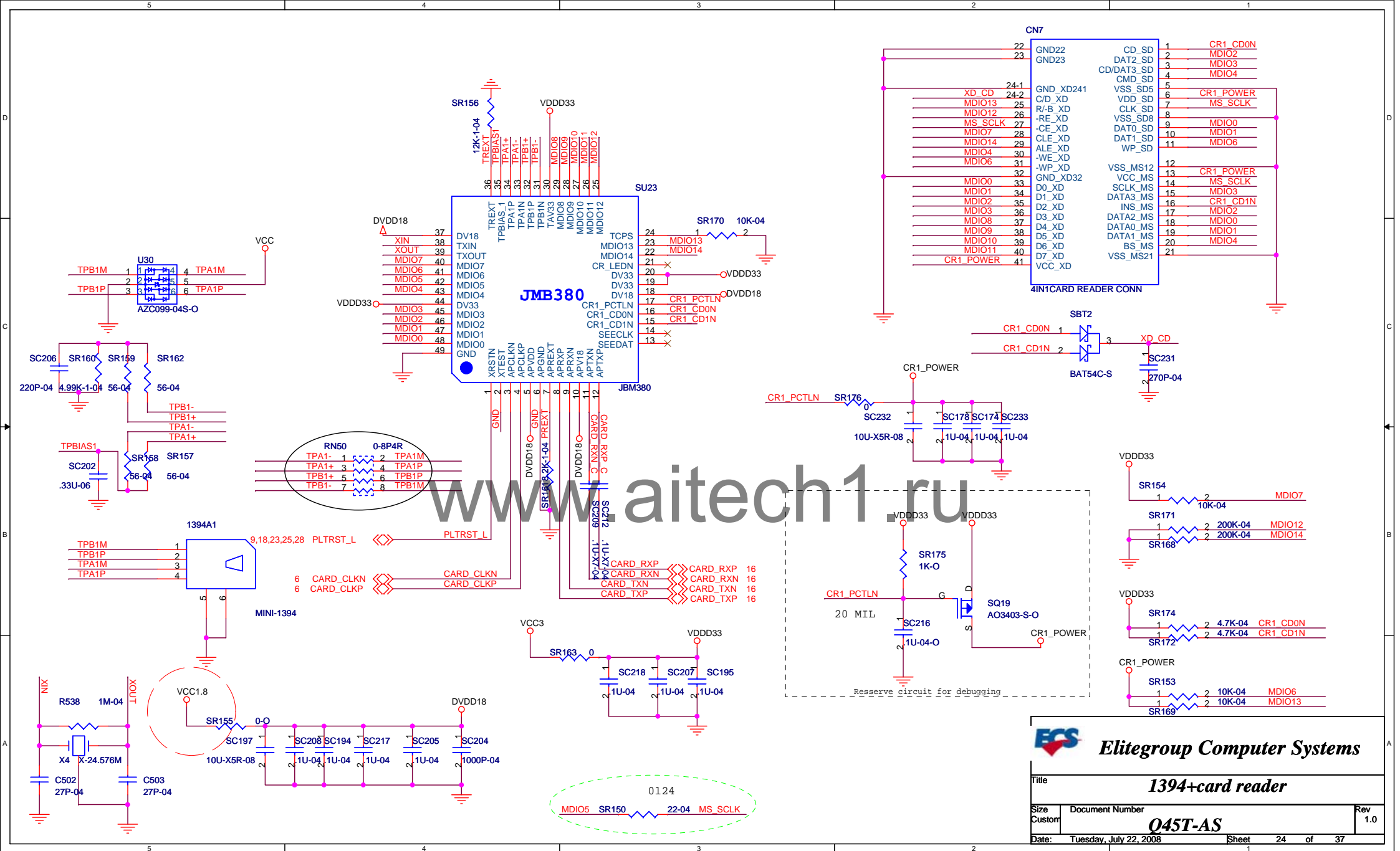
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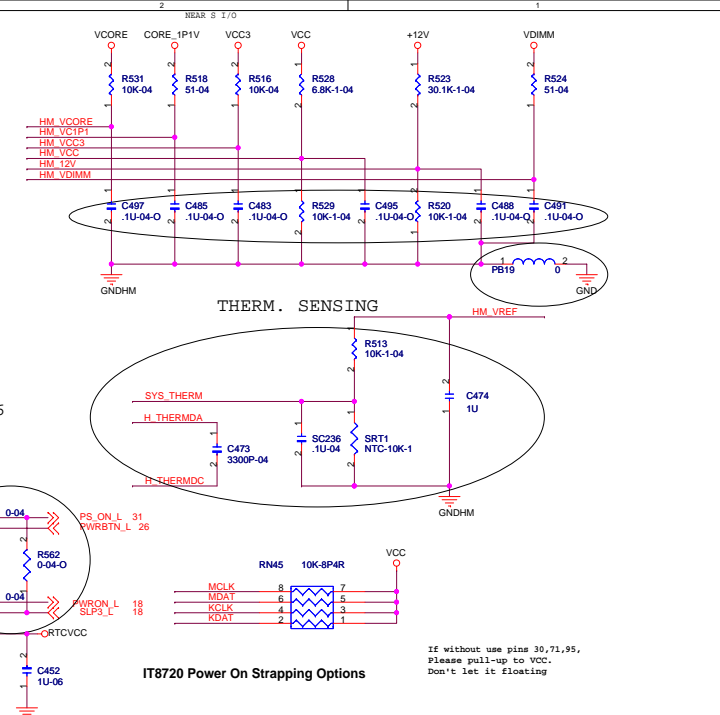


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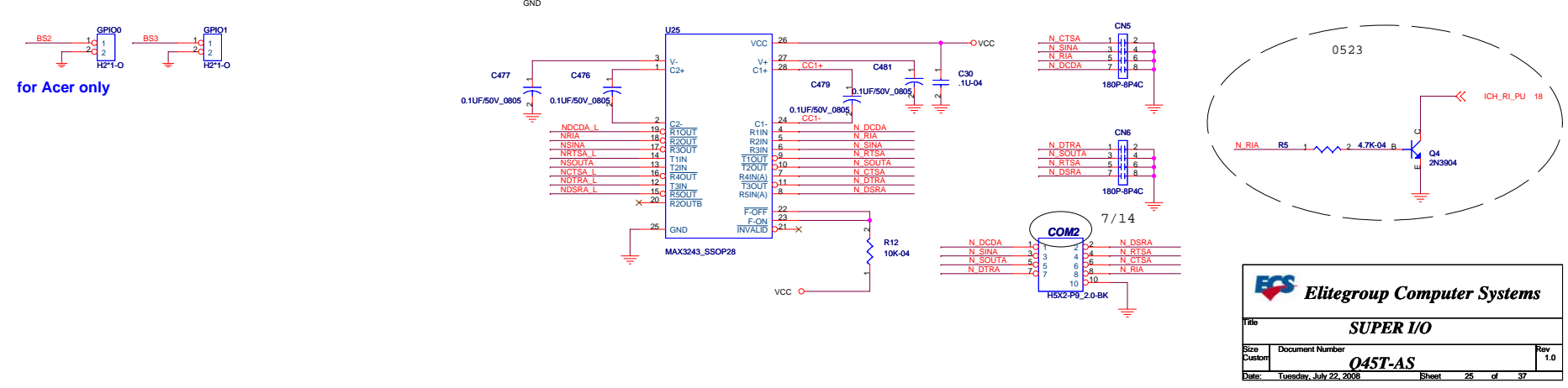




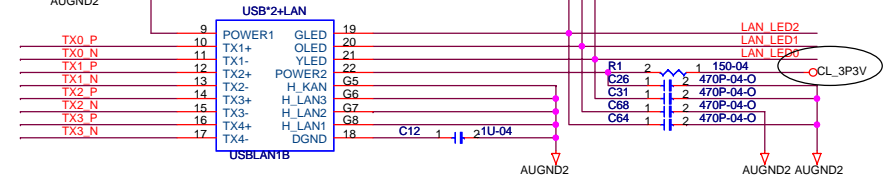
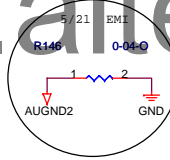
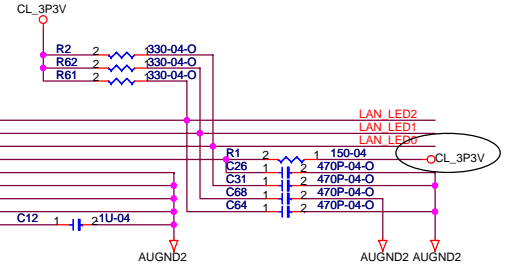
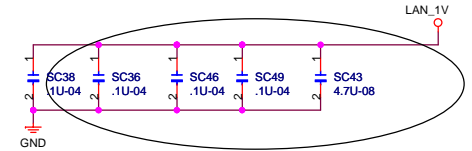
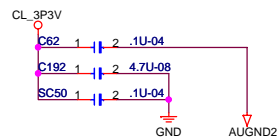




	Symbol	value	Description
JP1	FlashSeg1_EN	1	Disabled.
Pin 38		0	Flash I/F Address Segment 1 is enabled
JP2	VIDO_EN	1	Disable VID output pins
Pin 122		0	Enable VID output pins
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 126		0	K8 power sequence function is enabled
JP3	CHIP_SEL	11	Default Index 15h/16h/17h is 40h 50%
Pin 124 JP5		10	Default Index 15h/16h/17h is 7Fh 0%
Pin 46 JP6	FAN_CTL_SEL	01	Default Index 15h/16h/17h is 00h 100%
		00	Default Index 15h/16h/17h is 20h 75%
JP5	WDT_EN	1	Disable WDT to rest PWROK
Pin46		0	Enable WDT to rest PWROK
JP6	SVID_EN	1	Disable SVID Function
Pin29		0	Enable SVID Function



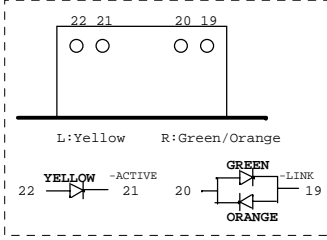
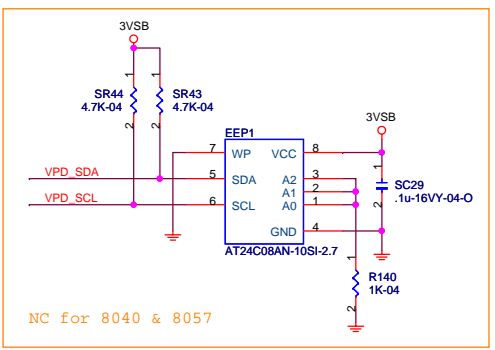



Giga PHY

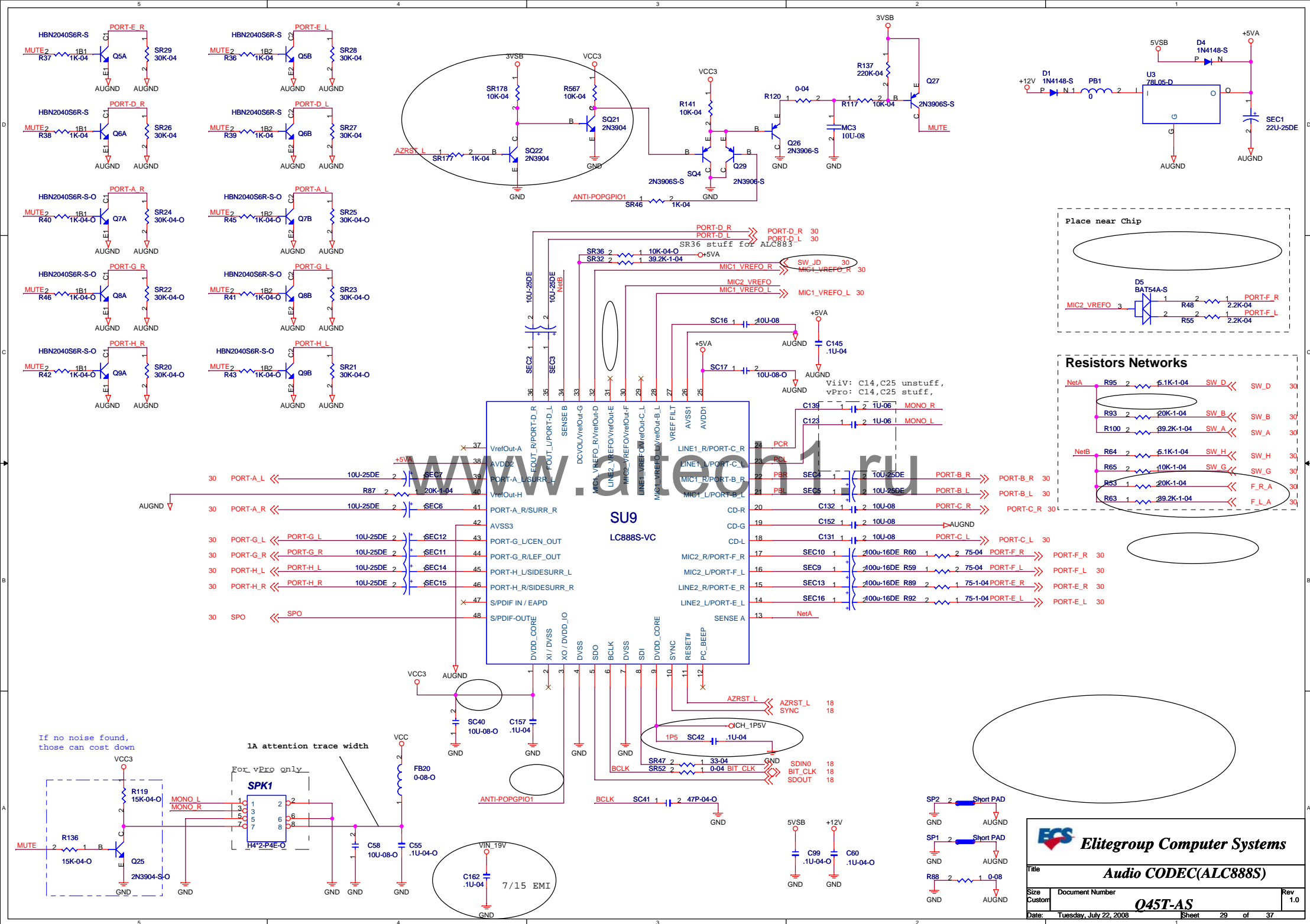
Wiring diagram for the 220V AC input. The diagram shows a transformer with primary terminals 22 and 21, and secondary terminals 20 and 19. The secondary is connected to a bridge rectifier with terminals labeled G (Ground), -LINK, and O (Output). The output is connected to a terminal block with terminals 22 (L:Yellow) and 21 (~ACTIVE).

For 10/100M Conn: 10-084-022232,  
10-084-022690, 10-084-022498  
For 1000M Conn: 10-084-022514 (ESD)

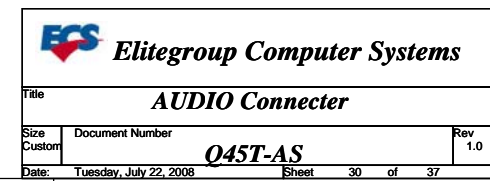
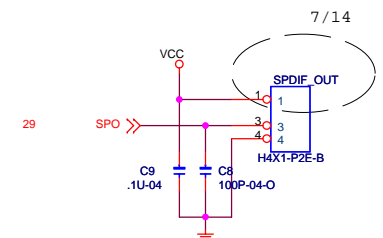
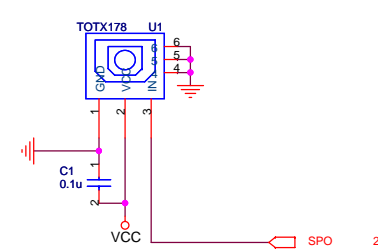
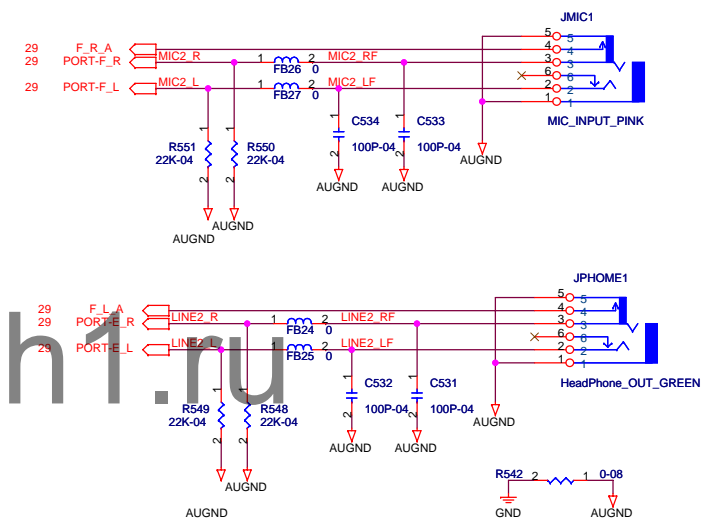
10-084-022503

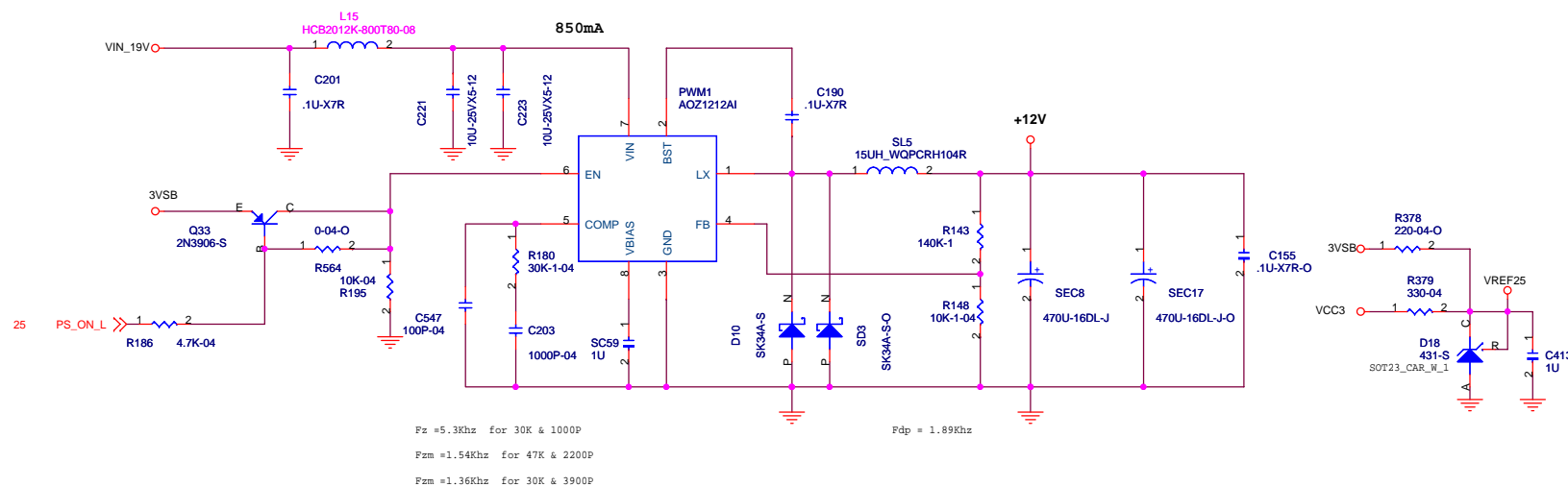


 <b>Elitegroup Computer Systems</b>			
<b>Title</b> <b>MARELL LAN:8070/75 DASH(Giga LAN)</b>			
<b>Size</b> Custom	<b>Document Number</b> <b>Q45T-AS</b>	<b>Rev</b> 1.0	
<b>Date:</b> Tuesday, July 22, 2008	<b>Sheet</b> 28	<b>of</b> 37	

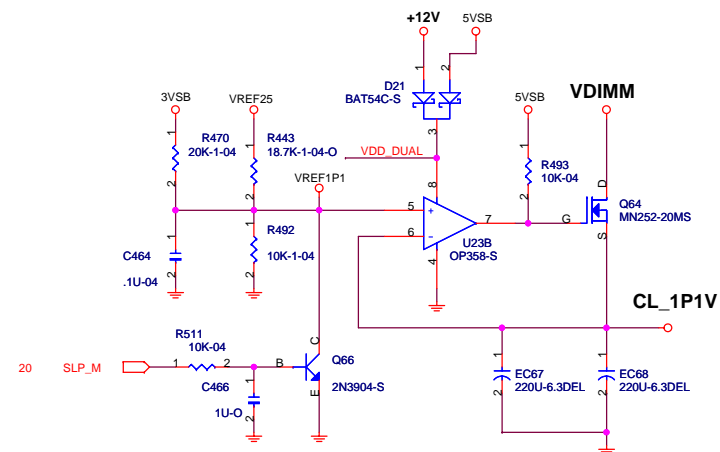
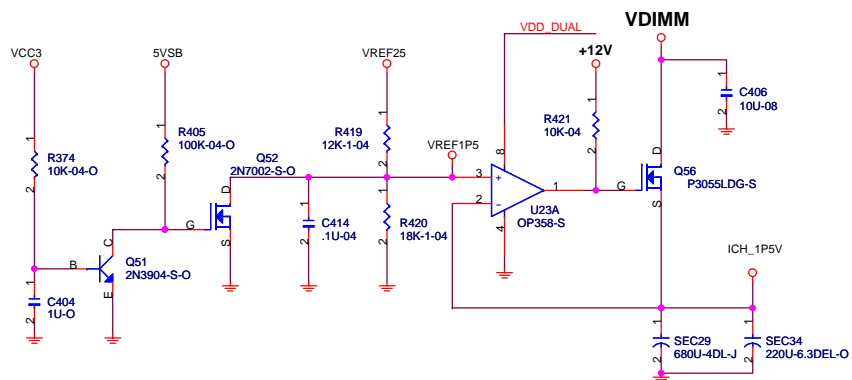




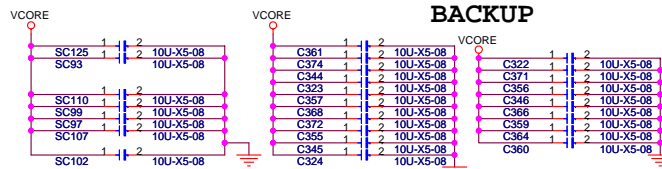
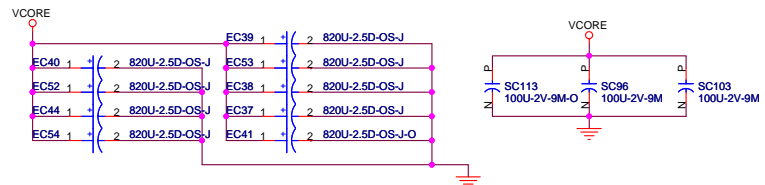
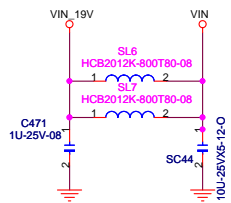
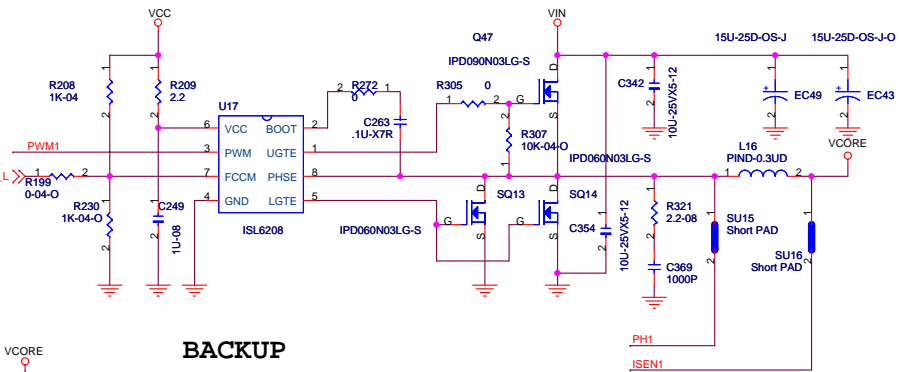
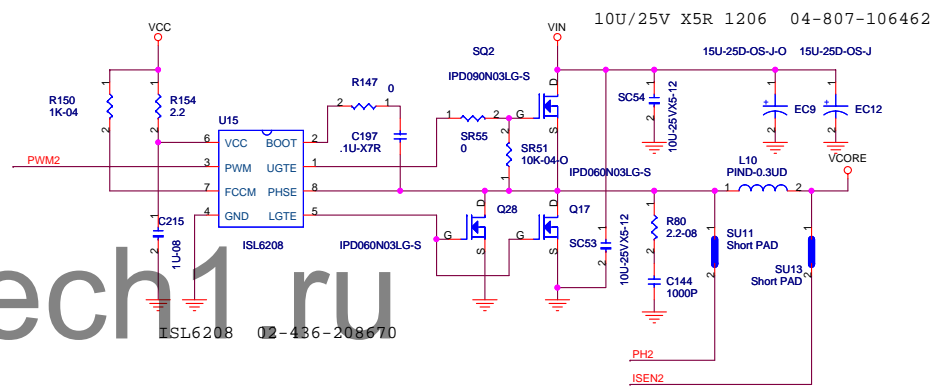
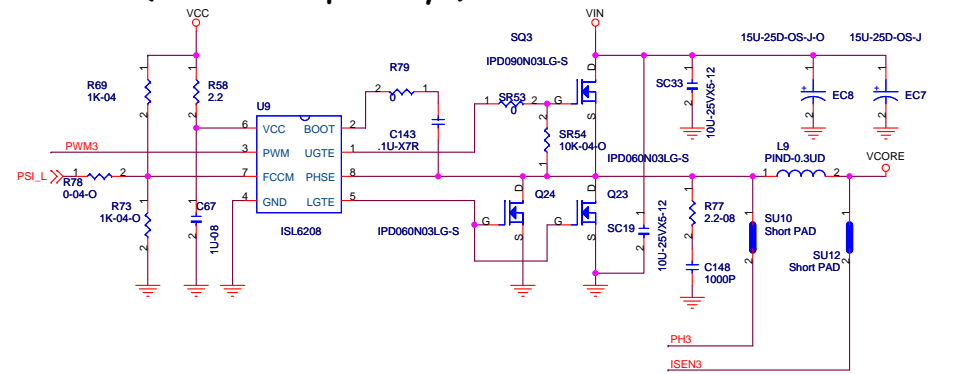
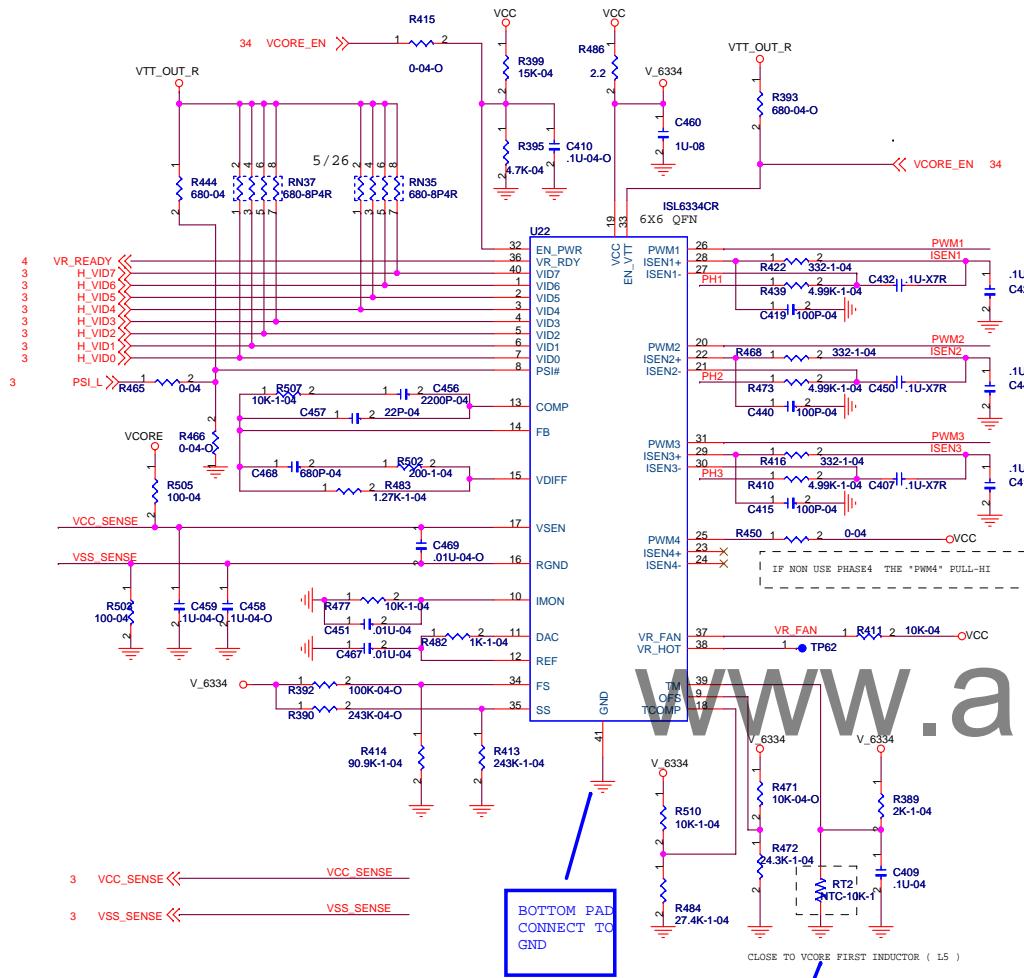




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## ISL6334CR FOR VRD11.1 POWER CKT ( Low frequency )



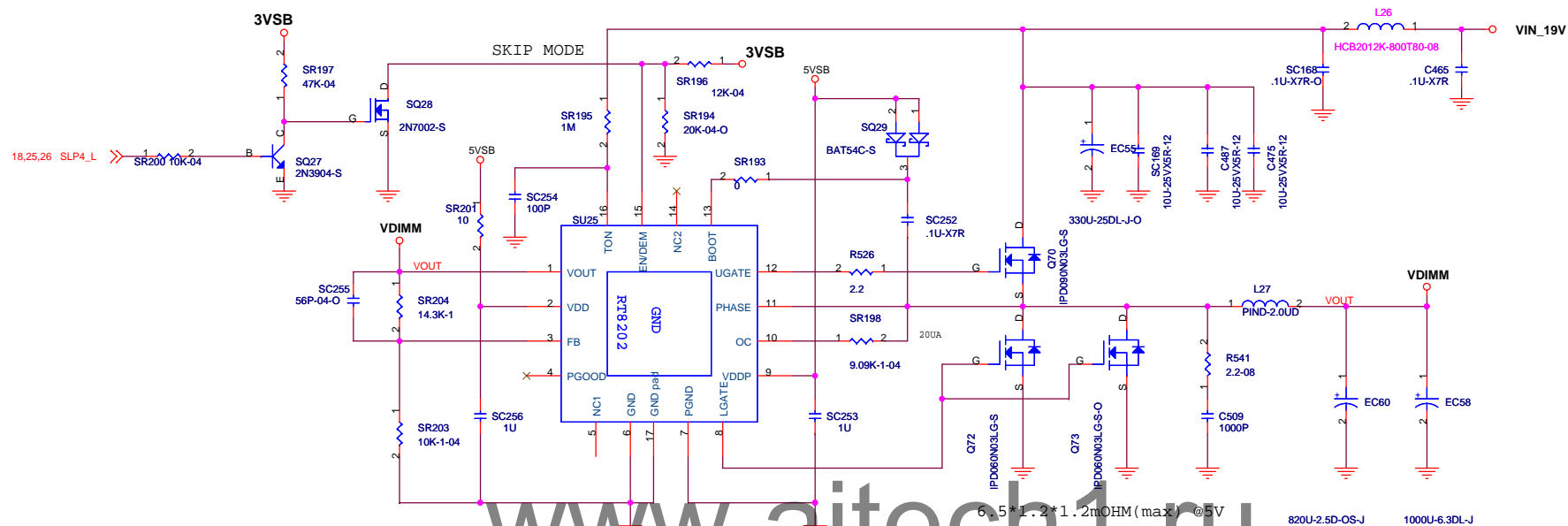
04-807-106192(10U-X5R-08-K)

## BACKUP

03-050-760363 (IPD060N03LG)

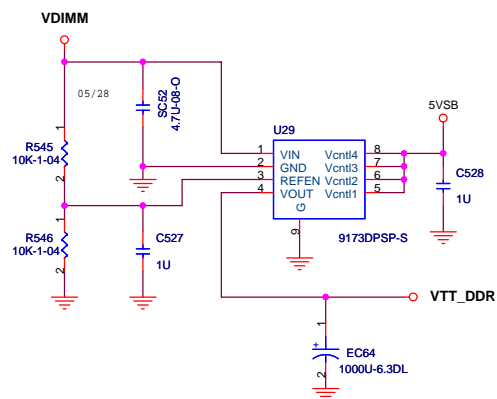






$$1.515V = 0.75V * (1 + 10.2K / 10K) 10a$$

$$1.830V = 0.75V * (1 + 14.7K / 10.2K)$$



3 TP\_HH4  
3 TP\_HN4  
3 TP\_HP5  
3 TP\_HAC4

TP\_HH4 1 STP39  
TP\_HH4 1 STP60  
TP\_HP5 1 STP53  
TP\_HAC4 1 STP59

7 TP\_MN25  
7 TP\_MAB13  
7 TP\_MAD13

TP\_MN25 1 STP31  
TP\_MAB13 1 STP68  
TP\_MAD13 1 STP67

17 TP\_SC18  
17 TP\_SE19  
17 TP\_SB16

TP\_SC18 1 STP12  
TP\_SE19 1 TP13  
TP\_SB16 1 STP10

18 TP\_SM2  
17 TP\_SM3  
18 TP\_SK2

TP\_SM2 1 STP5  
TP\_SM3 1 STP3  
TP\_SK2 1 STP2

18 TP\_SF20  
19 TP\_SH17  
19 TP\_SAC7

TP\_SF20 1 TP14  
TP\_SH17 1 TP10  
TP\_SAC7 1 TP9

17 TP\_SC19  
17 TP\_SA16

TP\_SC19 1 STP14  
TP\_SA16 1 STP11

27 TP\_LAN51  
27 TP\_LAN12  
27 TP\_LAN13

TP\_LAN51 1 TP5  
TP\_LAN12 1 TP3  
TP\_LAN13 1 TP2

3 TP\_HAB3  
3 TP\_HC23  
3 TP\_HAL8  
3 TP\_HAL7  
3 TP\_HF29

TP\_HAB3 1 STP71  
TP\_HC23 1 STP19  
TP\_HAL8 1 STP45  
TP\_HAL7 1 STP44  
TP\_HF29 1 STP8

9 TP\_MAR7  
9 TP\_MAN10  
9 TP\_MAN11  
9 TP\_MAN9

TP\_MAR7 1 STP82  
TP\_MAN10 1 STP60  
TP\_MAN11 1 STP79  
TP\_MAN9 1 STP81

3 TP\_HE29  
3 TP\_HAH2  
3 TP\_HV2  
3 TP\_HAA2

TP\_HE29 1 STP9  
TP\_HAH2 1 STP66  
TP\_HV2 1 STP76  
TP\_HAA2 1 STP75

9 TP\_MR15  
9 TP\_MR14  
9 TP\_MT15  
9 TP\_MT14

TP\_MR15 1 STP54  
TP\_MR14 1 STP47  
TP\_MT15 1 STP58  
TP\_MT14 1 STP55

4 TP\_HAK3  
4 TP\_HAJ4  
3 TP\_HA23  
3 TP\_HB23

TP\_HAK3 1 STP61  
TP\_HAJ4 1 STP72  
TP\_HA23 1 STP13  
TP\_HB23 1 STP18

9 TP\_MB14  
9 TP\_ML11  
9 TP\_MA45  
9 TP\_MB2  
9 TP\_MBE1  
9 TP\_MBE45  
9 TP\_MG15

TP\_MB14 1 TP20  
TP\_ML11 1 STP36  
TP\_MA45 1 STP25  
TP\_MB2 1 TP54  
TP\_MBE1 1 STP87  
TP\_MBE45 1 STP88  
TP\_MG15 1 STP29

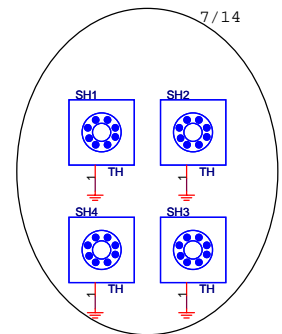
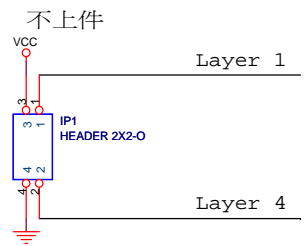
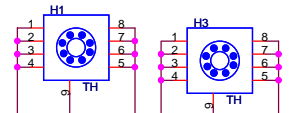
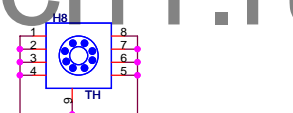
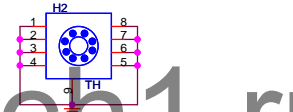
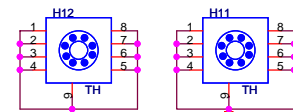
3 TP\_HG6  
3 TP\_HAL3

TP\_HG6 1 STP48  
TP\_HAL3 1 STP65

8 TP\_MAW37  
8 TP\_MAV35

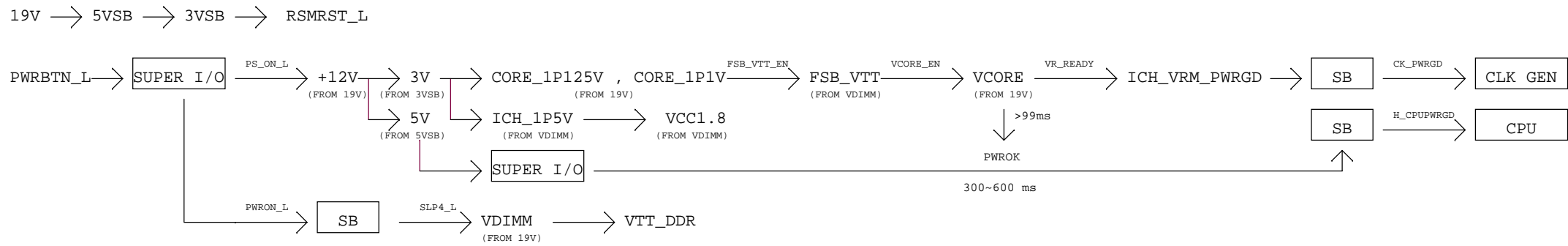
TP\_MAW37 1 STP84  
TP\_MAV35 1 STP85

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1080 : trace width 4 mil 50 ohm  
Trace Length 3150 mils  
Spacing: 1.clearance to itself 50/4/50(S:W:S)  
2.clearance to other signal 3W





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Title <b>POWER SEQUENCE</b>			
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